Analog Electronic Circuit Design

As per KL University Vijayawada Syllabus 2018-19

V Ramani Kumar
Prof (ECE) – KL University,
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About the book and the author………………..

Why I wrote (write?) this book?
There are so many books on Analog Electonic Circuit Design. Why one more?

I thought quite a lot about it.
I am from the Industry. I had worked in Telecom R&D for nearly 35 years (electronics, embedded and wireless).
I have been part of huge R&D teams of some of the best Telecom institutions of India

- *DRDO Bangalore, Gujarat communications Baroda, Escorts Telecom Delhi. Solidaire Chennai, Telecom Technology Ltd Hong Kong, Tata Telecom Chennai, Bharti Telecom, Delhi and Premier Evolvics, Coimbatore*

So what?
I had the fortune of working with hundreds of engineers everywhere ….fresh engineers straight out of the college. I had trained them in circuit designs, embedded designs and system designs. I understand the gap between the industry expectations and the academic objectives, better than many professionals or academicians.

I thought I am qualified enough to address this gap. I teach in Engineering colleges too and try my best to bring an Industry perspective into every lecture of mine. The students, as well as the faculty. seem to like this approach.

This encouraged(s) me to write a book on basic electronics first for VTU Bangalore and now on Analog Electronic Circuits Design for KLU Vijayawada. This maybe a one-stop-solution for a good book on AECD.
The approach is simple, bringing out the design issues at every opportunity, with an objective to make the student master the concepts.

Simple structured presentation of the syllabus, with plenty of illustrations, should help demystification of Analog electronics.

I dedicate this book to

> ***My wife Karpagam – For her great contribution in bringing out this book.***
> ***KLU family of Students - Vijayawada and Hyderabad***

This text book follows the KLU syllabus verbatim and is brought out in fewer than 200 pages. I am sure, the student world will welcome this.

My sincere and special thanks to President KL University, for encouraging me to write this book. As always, he is a great source of inspiration………………

Pls explore my animation videos at ***https://www.youtube.com/dashboard?o=U***

Good luck,

ramani kumar

AECD – Proposed new syllabus

Diodes: Diode theory, forward and reverse-biased junctions, reverse-bias breakdown, load line analysis, diode applications - Limiters, clippers, clampers, voltage multipliers, half wave & full wave rectification, Capacitor filters, ripple factor, Zener diode,. Regulators: Series and shunt voltage regulator,

Transistors: Q point, Self-Bias-CE, h-model of Transistor, Expression of voltage gain, current gain, input & output impedance, Emitter follower circuits, High frequency model of Transistor, FET fundamentals, Configurations, current-voltage characteristics, parameters of JFET, Biasing of JFET, Biasing of MOSFET. RC coupled amplifier and analysis, FET small signal model, Concept of Feedback, Feedback amplifier configurations.

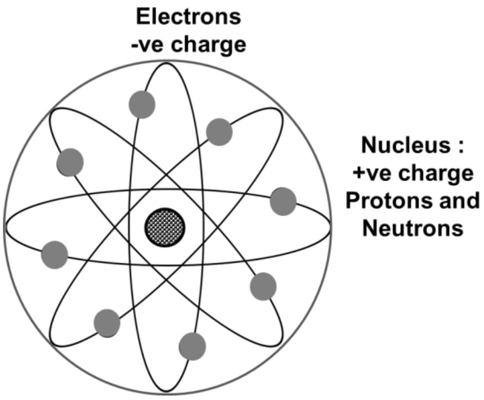
Op-amps: Ideal OPAMP, Concept of differential amplifier, CMRR, Open & closed loop circuits, importance of feedback loop (positive & negative), inverting & non-inverting amplifiers, Voltage follower circuits. Adder, Integrator & Differentiator, Comparator, Schmitt Trigger, Instrumentation Amplifier. Filter Circuits**:** Analysis of Low pass, High pass, Bandpass, Band reject,

Oscillators: Barkhausen criterion, Colpitt, Hartley's, RC Phase shift, Wien bridge, & Crystal oscillators.

555 applications: Monostable & Astable operation using 555 timers

Chapter 1: Semiconductor Theory

1.1 ATOM –Structure



- Atom consists of a nucleus. Electrons in several orbits move around the **nucleus**..
- Contains three basic Particles –**Protons, Neutrons & electrons.**
- Nucleus contains two types of particles
  - **Protons :** Positively charged particles.
  - **Neutrons :** Particles with neutral charge.
- **Electrons:** Negatively charged particles (Charge = 1.602X 10^{-9} Coulombs).

Fig 1.1 Atom - Structure

Usually protons and electrons will be equal in number .Therefore, atoms are normally neutral, electrically.

- If an atom loses an electron, it means that it has lost some -ve charge & hence has a net + ve charge ……….. and vice versa.

1.1.1 Holes & Electrons (Silicon & Germanium)

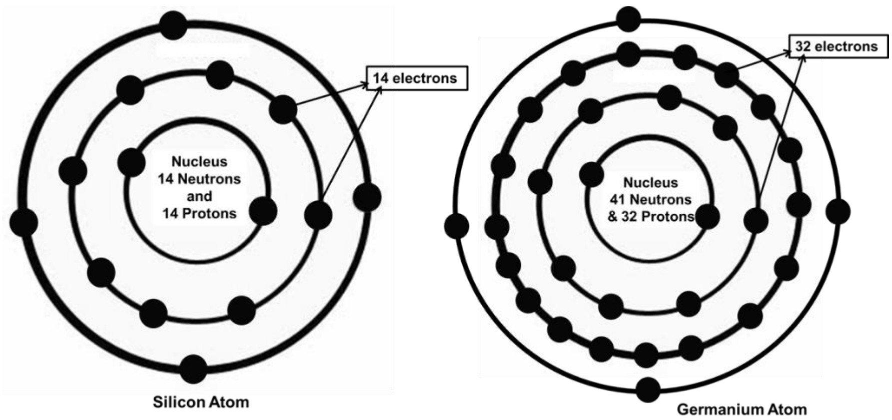


Fig 1.2

Pls recall,

1. Electrons can occupy only some fixed orbits, called **shells**.
2. Each shell can be occupied by only some **specific number of electrons**.
3. The outer most shell called **valence shell**, may be only partially filled by electrons.
4. Figure 1.2 gives a 2 D simplified orbital arrangement of silicon & germanium atom.
5. Absence of an electron in a shell, is defined as a **hole**.
6. Silicon & Germanium atoms are **electrically neutral (outer shell has 4 holes and 4 electrons each**)

1.2 Electron & Hole Dynamics

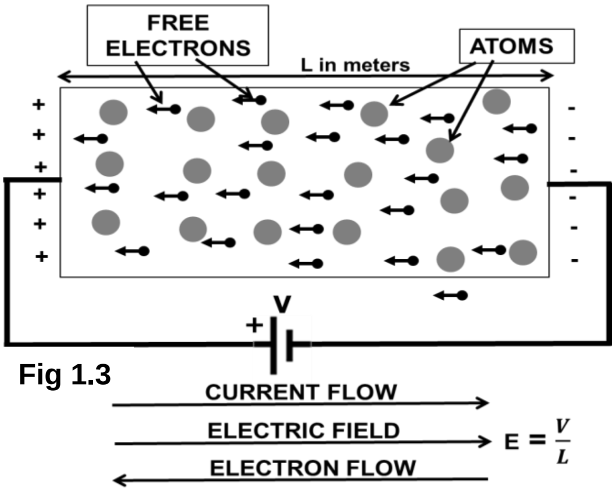


Fig 1.3

Refer fig 1.3.

- **Electrons** are –vely charged particles. Electrons are **repelled by –ve voltage**. Therefore, they will move towards a terminal **where + ve voltage is applied**.
- **Holes** are **+vely charged** particles. Holes are repelled by + ve voltage. They will move towards a terminal **where -ve Voltage is applied**.
- Please note the direction of the current flow is **always opposite** to the direction of electron flow.

1.3 N type & P type Semiconductors

1.3.1 Intrinsic semiconductor: It is very pure chemically. It has **equal numbers of** electrons (-ve) and holes (+ve). It has **poor conductivity.**

1.3.2 Extrinsic semiconductor:

- When a **small amount, of impurity is added** to a pure semiconductor, the conductivity of the semiconductor is increased manifold.
- Such materials are known as extrinsic semiconductors.
- The deliberate addition of a **desirable impurity**, is called **doping.**
- Doping yields two types of semiconductors viz p type and n type.
- The impurity atoms are called **dopants.**
- Such a material is also called a **doped semiconductor.**
- **Silicon & Germanium** are the standard semiconductor atoms, used by the industry.

Some of the popular dopants used, in doping the tetravalent Si or Ge are,
Trivalent atoms such as Boron or Aluminium, for producing p type semiconductors.
Pentavalent atoms such as Arsenic or Phosphorous, for producing n type semiconductors.

n type: Refer fig 1.4. **Pentavalent (5)** impurities like Arsenic (As), Antimony (Sb), Phosphorous (P), when added to either silicon or germanium, will produce N type semiconductors. **Electrons are the majority carriers**.

p type: Refer fig 1.5. **Trivalent (3)** impurities like Indium (In), Boron (B), Aluminium (Al) when added to either Silicon or Germanium, will produce P type semiconductors. **Holes are the majority carriers**.

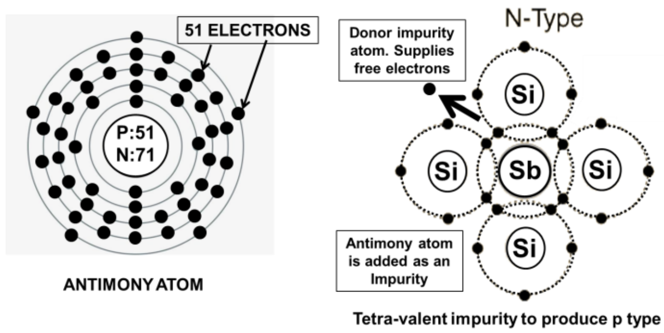


Fig 1.4 n-type pentavalent atom

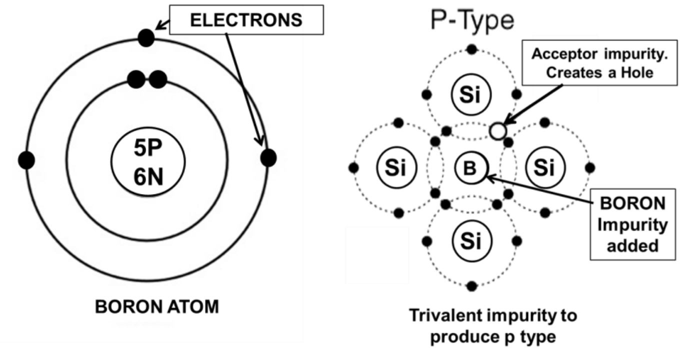


Fig 1.5 p-type trivalent atom

Majority and minority carriers

Majority carriers:

- The more abundant charge carriers
- Primarily responsible for current transport in a semiconductor.
- n-type semiconductors: Electrons
- p-type semiconductors: Holes.

Minority Carriers:

- The less abundant charge carriers
- n-type semiconductors: Holes
- p-type semiconductors: Electrons.

1.4 pn junction

Figure 1.6 shows independent p type independent n type semi-conductor.

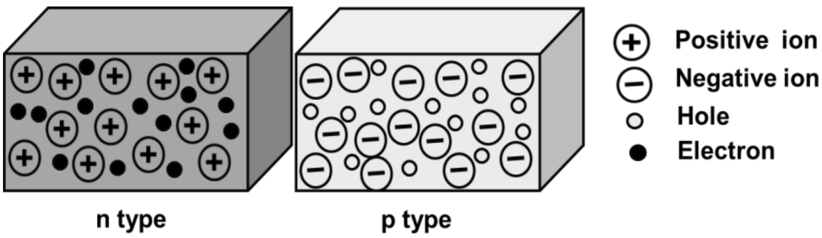


Fig 1.6 Semiconductor material n-type and p-type

Fig 1.7 shows a p type and n type conductor joined together (fabricated) to form a p-n junction

- There is no external voltage (bias) applied.
- Initially, pn junction is electrically neutral.

- **Majority carriers of n type are electrons.**
- **Majority carriers of p type are holes.**

1.4.1 Diffusion

Refer fig 1.7. Due to thermal agitation, electrons and holes start moving randomly, even if there is no bias. Look at the diffusion process below.

Few electrons close to the junction, start crossing the junction, to reach p side	Few holes close to the junction, start crossing the junction, to reach the n side
These electrons combine with some holes in the p side, to create some –ve ions.	These holes combine with electrons in the n side to create some +ve ions.
Due to these ions, a -ve voltage build up (barrier) is created, on the p side.	Due to these ions, a +ve voltage build up (barrier) is created on the n side.

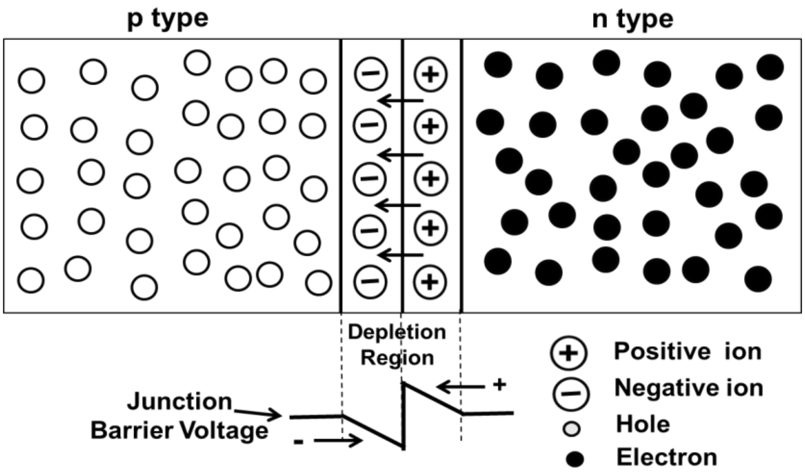


Fig 1.7 p-n junction diode – No bias voltage

This barrier voltage build up is shown in the figure 1.8.

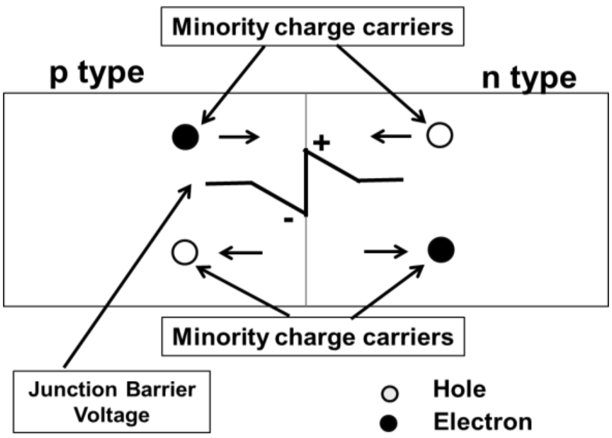


Fig 1.8 Barrier Voltage at p-n junction

- Barrier voltage is typically **0.7 V, for Silicon**.
- Barrier voltage is typically **0.3 V, for Germanium.**
- At around the barrier voltage, **electrons (from n side) are repelled by the – ve barrier voltage in the p side.**
- At around the barrier voltage**, holes (from p side) are repelled by the +ve barrier voltage in the n side.**
- Therefore further diffusion stops.

1.4.2 Depletion region

- In the diffusion process mentioned above, **when the barrier potential is reached, further diffusion stops.**
- No charge carriers (electrons or holes) will be present, closer to the junction.
- Only ionized atoms (+ve and –ve), will be present on either side of the junction.
- This region is known as **depletion region**.

1.5 pn junction biasing

1.5.1 Reverse biased p-n junction

Refer figure 1.9.

What is reverse bias?

An external dc voltage (bias) is applied to a diode such that, p side is connected to the –ve terminal and n side is connected to the +ve terminal of a battery.

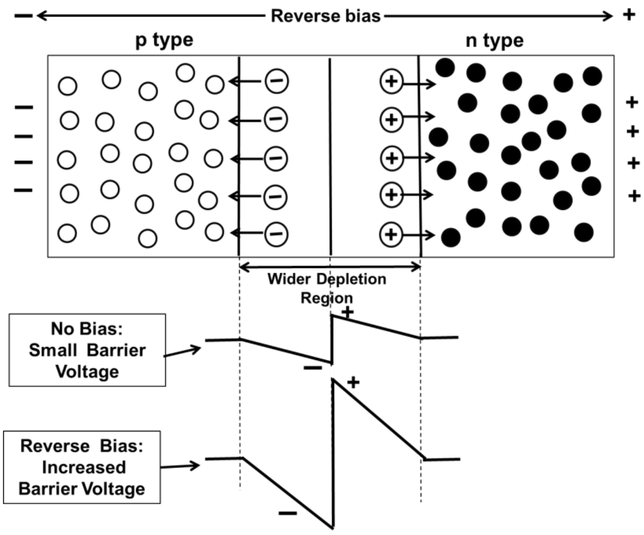


Fig 1.9 Reverse biased p-n junction

- This biasing arrangement increases the barrier voltage, as shown in the figure.
- Barrier voltage at n, becomes more +ve and the barrier voltage at p becomes more –ve.
- Electrons (majority carriers) in the n side, are repelled away from the junction and are attracted towards the +ve terminal.
- Holes (majority carriers) in the p side, are repelled away from the junction, and are attracted towards the –ve terminal.
- Consequently, depletion region further widens and barrier voltage increases as shown.

Result: Majority carriers cannot flow across junction and therefore, under reverse bias conditions, no current flow is possible. In other words, forward current does not flow.

1.5.2 Forward biased p-n junction

Refer figure 1.10.

What is forward bias?

An external dc voltage (bias) is applied to a diode such that **n side is connected to the – ve terminal and p side is connected to the +ve terminal of a battery.**

- This biasing arrangement decreases the barrier voltage, as shown in the figure 1.10.
- Barrier voltage at n, becomes less +ve and the barrier voltage at p becomes less –ve.
- Electrons (majority carriers) in the n side, are attracted across the junction, **towards the p side and are attracted towards the +ve terminal.**
- Holes (majority carriers) in the p side, are attracted across the junction, **towards the n side and are attracted towards the –ve terminal.**

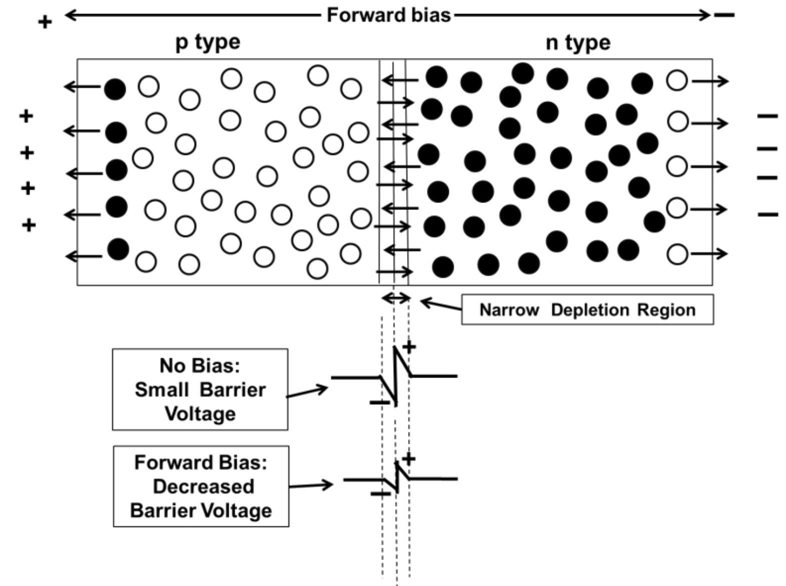


Fig 1.10 Forward biased p-n junction

- Consequently, depletion region decreases and the barrier voltage also reduces, as shown.

Result: Majority carriers will flow across junction and therefore, under positive bias conditions, current flow is possible. In other words, forward current flows.

Chapter 2: Semiconductor Diodes and Applications

2.1 p-n junction diode

What is a diode?

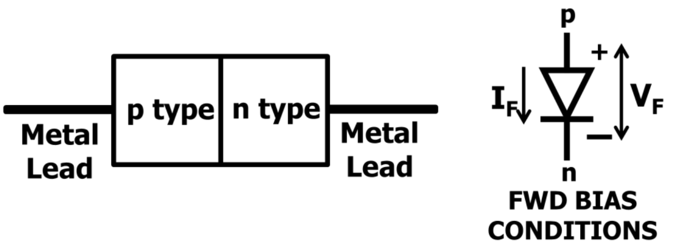


Fig 2.1 Semiconductor diode with leads

Draw the circuit symbol and indicate current flow.

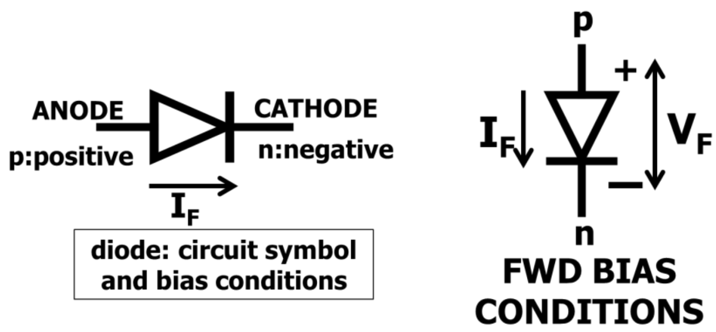


Fig 2.2

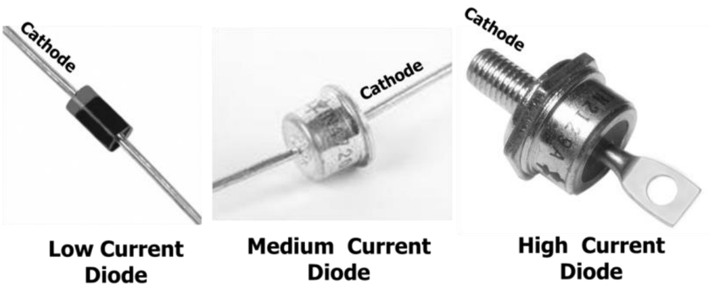


Fig 2.3

Refer fig 2.1 and 2.2

- It is a semiconductor device with a p-n Junction.
- It is a one way device.
- Allows current to flow when forward biased (p: + ve and n: -ve).
- Almost totally blocks current flow when reverse biased (p: - ve and n: +ve).
- Therefore, a diode is a 2 terminal component.
- It has two electrodes called anode and cathode.
- Anode is attached to p side and cathode to n side.

Diodes Power classification: Refer fig 2.3.

- **Low power diodes:** Usually small diodes can handle low currents up to 100mA. Power dissipation will be less than 800 milli-watts.
- **High power diodes:** Large diodes can handle high currents (1 to 10 Amperes). Power dissipation will be between 1 watt and 10 watts.
- Look at the table below

Diode size	Cathode Identification	Forward current (mA)	Reverse voltage (V)
Small-	Color band or dot	100	75
Medium	Diode Symbol	400	200
Large	Threaded portion	Few amperes	Few hundreds

2.2 Characteristics and parameters:

2.2.1 Diode characteristics: Refer fig 2.4 and 2.5

- It is the study of, ‘voltage-across-the-diode’ versus ‘current- through-the-diode’.
- As we know, diode is a p-n junction semi-conductor device.

- When it is **forward biased**, diode characteristics is a **study of forward voltage (or threshold voltage) V_F & forward current I_F.**
- When it is **reverse biased**, the diode characteristics is a study of reverse voltage **(or threshold voltage) V_R & reverse current I_R**.

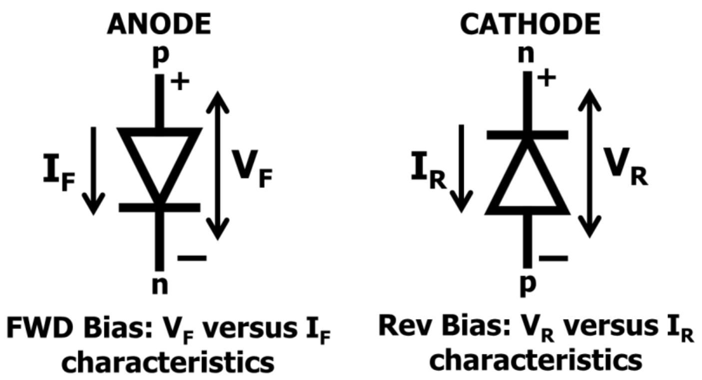


Fig 2.4

2.2.2 Diode equation

Current contribution in Diode is due to majority charge c
exponentially increases with applied voltage as given diode equation by

$$I = I_0\left(e^{\frac{v_d}{\eta\, V_T}} - 1\right) \approx I_0 e^{\frac{v_d}{\eta\, V_T}}.$$

I	Current through the diode, in Amps
v_d	Diode voltage with the anode positive with respect to the cathode, in V
I_0	Leakage (or reverse saturation) current.
η	empirical constant known as the emission coefficient or the ideality factor**.**
V_T	Voltage equivalent of temperature (= kT/q**)**

2.2.3 Forward characteristics (Silicon): Refer fig 2.5

Up to 0.7 V

- As the forward bias is increased from **0.1 to 0.7 V**, the diode hardly conducts the **forward current is very low** (less than 5 mA).

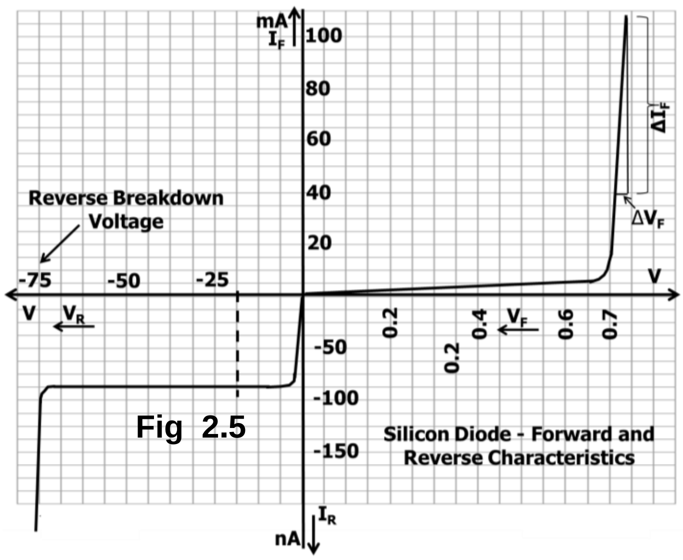


Fig 2.5

Beyond 0.7 V

- As the forward bias is increased **beyond 0.7 V**, the **forward current increases** very sharply.
- Increasing the **forward bias beyond say 1.0 V, will destroy a diode** due to excessive forward current.
- A **current limiting resistor is needed** in the circuit to protect the diode.

2.2.4 Reverse characteristics (Silicon)

0 to -75 V

- Please **note the change of scale, in the y axis between forward & reverse characteristics**.
- **Reverse current I_R, is often very low** (not more than 1 μA) for reverse voltages up to -75 V for silicon
- **I_R is negligible compared to I_F.**

- For all practical purposes the diode behaves like an open circuit.

Beyond -75 V:

- **Reverse break down** happens (we shall study this later).
- The current **increases abruptly**.
- This **can destroy the diode**, unless protected by a **current limiting resistor**
- **Peak Inverse Voltage (PIV):** The maximum reverse-bias voltage that a diode can withstand without "breaking down" is called the **Peak Inverse Voltage, or PIV rating**.

2.2.5 Diode characteristics (germanium)

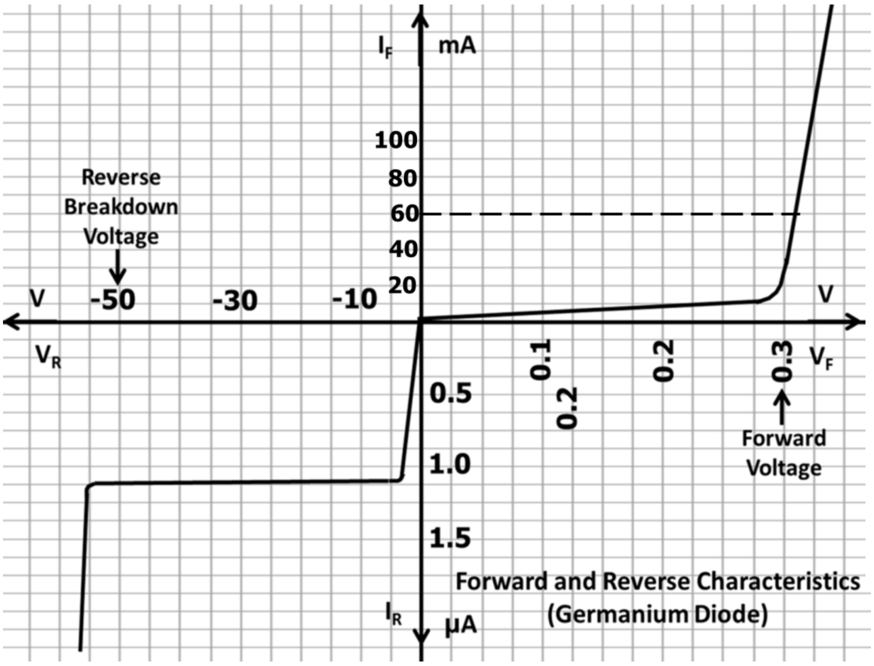


Fig 2.6 Germanium diode – Fwd and Rev characteristics

Refer fig 2.6.

- The characteristics are similar to that of silicon diode.
- Forward voltage is 0.3 V instead of 0.7 V.
- Reverse break down voltage is -50 V instead of -75 V.
- Reverse current is -1.0 μA instead of -100 nA.

2.2.6 Variation of forward voltage (Threshold voltage) with temperature

We know, Silicon diode has a forward voltage of is 0.7 V at 25°C and Germanium diode has a forward voltage of is 0.3 V at 25°C

Temp Coefficient of Silicon is given by $K_{TC(Silicon)}$ = - 2 mV / °C.

Temp coefficient is negative, meaning that forward voltage decreases as temperature increases.

Find the threshold voltage at 100°C for Germanium and Silicon.

Ans: 0.15V and 0.55V

2.2.7 Reverse bias break down mechanism

<u>Case 1</u>

<u>Very narrow depletion region</u>

- **Reverse voltage produces very high field strength**.
- What is field strength? Voltage per distance **(Volts / Distance.)**
- **Electrons break away from their atoms due to this field strength**.
- $\therefore$ Due to this electron flow, depletion region is converted into a conductor (from insulator)
- This is called **ionization by electric field**
- This is known as Zener break down mechanism
- Usually occurs when **reverse bias is < 5V**

<u>Case 2</u>

<u>Depletion region very wide</u>

- In the reverse bias mode reverse saturation current flows.
- There are electrons moving in reverse saturation current.
    - **When these electrons travel in the wide depletion region, these electrons gain a lot of energy**
    - These energetic electrons **collide with atoms** and cause their **electrons to break-free**.
    - Due to these new electrons, **more collisions** occur and more electrons get released
- This is known as **Avalanche break-down**.
- Also known as **Ionization by collision**
- Usually occurs when **reverse voltage is > 5V**

2.2.8 What is reverse saturation current (ICO)?

Occurs during reverse bias conditions

When a diode is reverse biased, we know the depletion region width increases.

Therefore no current flow happens due to majority carriers

However minority carriers diffuse through this depletion region

In a PN junction diode, the reverse saturation current occurs due to diffusion flow of electrons (minority carriers) from p region to n region and flow of holes (minority carriers) from n region to p region.

This current is nearly constant and is known as **reverse saturation current ICO**

2,2,9 How does reverse saturation current (ICO) behave with temperature?

Reverses saturation current is a nuisance.

It **increases** rapidly with temperature.

The increase is of the order of 7%/ºC for both germanium and silicon

In other words ICO doubles for every 10ºC rise in temperature and is definitely serious.

$\mathbf{I_2 = I_1 * 2^{\frac{(T2-T1)}{10}}}$ (I_2 = Current at new temperature and I_1 = Current at old temperature)

2.2.10 Forward & Reverse resistance : Refer fig 2.7

Problem 2.1: In fig 2.6, calculate the forward resistance of the germanium diode, at I_F= 60mA

At I_F = 60 mA, V_F = 0.33 V (approx)

Therefore, forward resistance

(R_F) = $\frac{\mathbf{V_F}}{\mathbf{I_F}} = \frac{0.33\ V}{60\ mA}$ = 5.5 ohms.

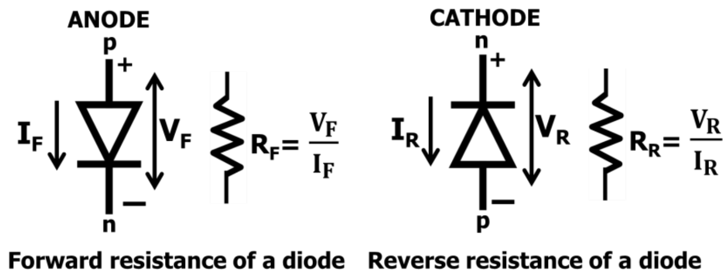


Fig 2.7

Problem 2.2: In fig 2.5, calculate the reverse resistance of the silicon diode at V_R =20V.

At V_R = 20 V, I_R = 90 nA (approx)

Therefore, reverse resistance (**R_R**) **=** $\frac{\mathbf{V_R}}{\mathbf{I_R}} = \frac{20\ \mathrm{V}}{90\ \mathrm{nA}}$ = 222 Mega ohms (approx)

2.2.11 Some of the important diode parameters.

V_F - Forward voltage drop (0.3 V for Ge and 0.7 V for silicon).

I_F - Forward current .

V_R - Reverse voltage.

r_d - Dynamic resistance = $\frac{\mathbf{\Delta V_F}}{\mathbf{\Delta I_F}}$

V_{BR} - Break down voltage {50 V for Ge and 75 V for Si).

P_D - Power dissipation.

2.2.12 Dynamic resistance r_d

Recall the forward resistance that was calculated in problem 2.1. **R_F =** $\frac{\mathbf{V_F}}{\mathbf{I_F}}$**.** This is the **DC resistance** of the diode, at one particular value of forward current. When the input varies by ΔV_F, there will be large variation, in forward current (ΔI_F). This is shown in fig 2.5

Dynamic resistance $\mathbf{r_d} = \frac{\mathbf{\Delta V_F}}{\mathbf{\Delta I_F}}$. r_d is also known as ac resistance or incremental resistance

There is another way of calculating dynamic resistance. It is not discussed here since it is beyond the scope of this book.The formula is $\mathbf{r_d} = \frac{\mathbf{26\ mV}}{\mathbf{I_F}}$

Problem 2.3: What is the dynamic resistance of a diode with a forward current of 5 mA

$\mathbf{r_d} = \frac{\mathbf{26\ mV}}{\mathbf{5\ mA}}$ = 5.2 Ω.

Problem 2.4: For the dynamic characteristic shown in fig 2.8, determine the dynamic resistance at 40 mA.

I_F = 40 mA.

Therefore, take a small interval around 40 mA as ΔI_F, say from 20 mA to 60 mA.

ΔV_F for this range = 0.726 V - 0.71 V = 0.016 V

ΔI_F for this range = 60 mA - 20 mA = 40 mA

$\therefore r_d = \frac{\Delta V_F}{\Delta I_F}, \quad = \frac{0.016V}{16\ mV} \quad = 0.4\ \Omega$

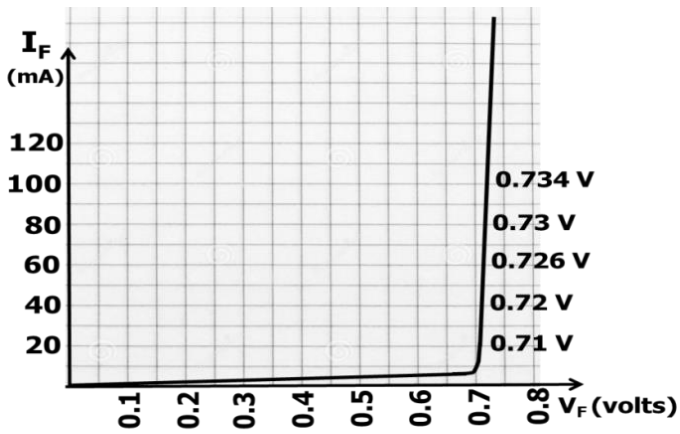


Fig 2.8

2.3 Diode approximations:

2.3.1 Ideal Diode:

Refer fig 2.9 a

In the forward bias condition

It will have no forward resistance and will not drop any voltage across it. **R_F = 0 Ω and V_F = 0 V.**

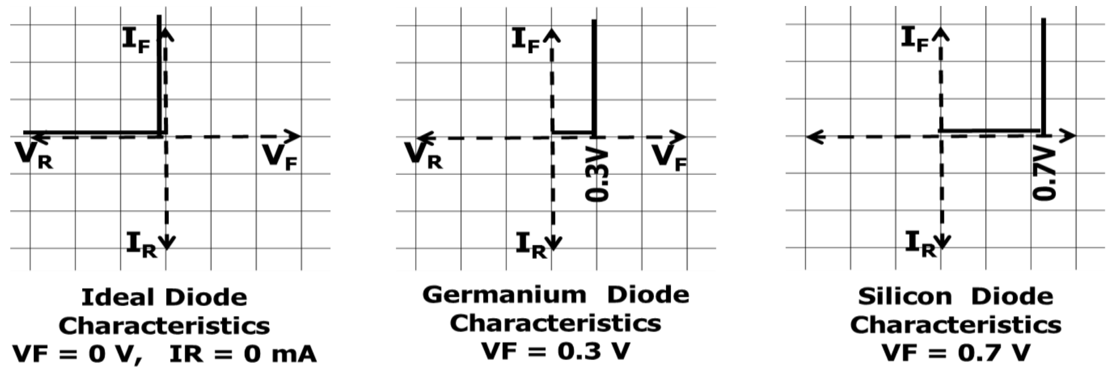
In the reverse bias condition, an ideal diode will never have any reverse current, no matter what the reverse voltage is. **$V_R = \infty$, $I_R = 0$**

Therefore, what is an ideal diode?

1. Fwd Resistance = 0 Ohm
2. Fwd Voltage drop = 0 V
3. Rev resistance = Infinity
4. Rev current = 0 amp

Refer fig 2.9 b and 2.9 c

However, in practice, it is different as seen already in figures 2.5 and 2.6.



(a) **(b)** **(c)**

Fig 2.9 Diode Characteristics

What are the assumptions of a near ideal diode (Si)?

Fwd Voltage drop = constant

Rev current = negligible (can be ignored)

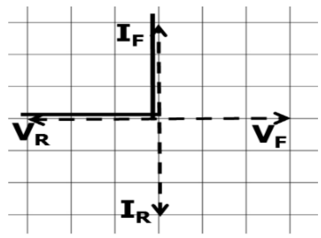
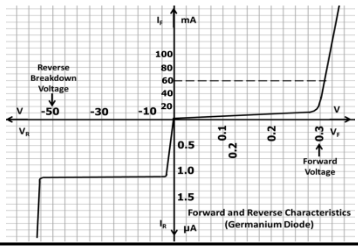
2.3.2 Practical diode

What is a practical diode (Si)?

Fwd Resistance = 0 to 20 Ohms

Fwd Voltage drop = 0.6 to 1.0 Volt

Rev current = few micro amps

Diodes Comparison		
Characteristic	**Ideal**	**Practical**
Threshold Voltage	No Threshold Voltage (0V)	Ge:0.3V, Si=0.7V
Forward current	Infinite if Vin > 0V	Finite
Forward Resistance	Zero	Finite
Reverse Resistance	Infinite	Large but finite
Breakdown Voltage	No Breakdown	Finite and depends on Doping
V-I Characteristic		

2.3.3 Piece-wise approximation of a diode

The smooth diode curve of fig 2.5 or 2.6 can be approximated by taking samples at very close intervals and interconnecting adjacent samples through short straight lines.

Problem 2.5: Construct a piece wise linear characteristics of a germanium diode, given that its dynamic resistance is 0.6 Ω and forward current is 100 mA .

Look at fig 2.10

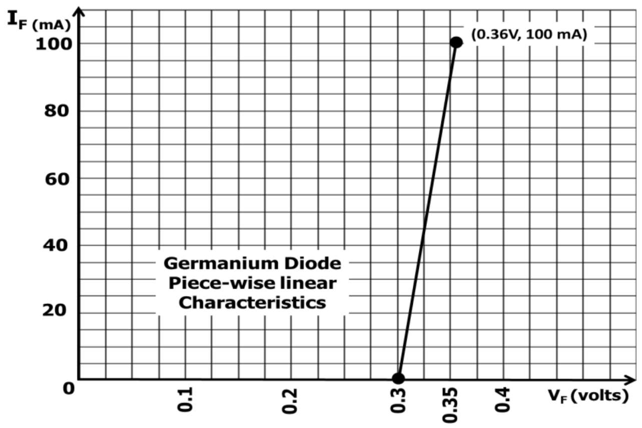


Fig 2.10

It is a Ge diode. V_F = 0.3 V

Mark Point A = (0.3 V, 0 mA)

How to find B?

ΔI_F = 100 mA – 0 mA = 100 mA

ΔV_F = ΔI_F X r_d

= 100 mA X 0.6 Ω = 60 mV.

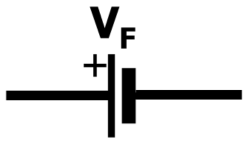
= 0.06 V

Point B = {(0.3 V + 0.06 V), 100 mA)}

= **{(0.36 V, 100 mA)}**

Join A B. The piece wise linear characteristic is the thick line segment shown.

2.3.4 DC equivalent circuits of a diode



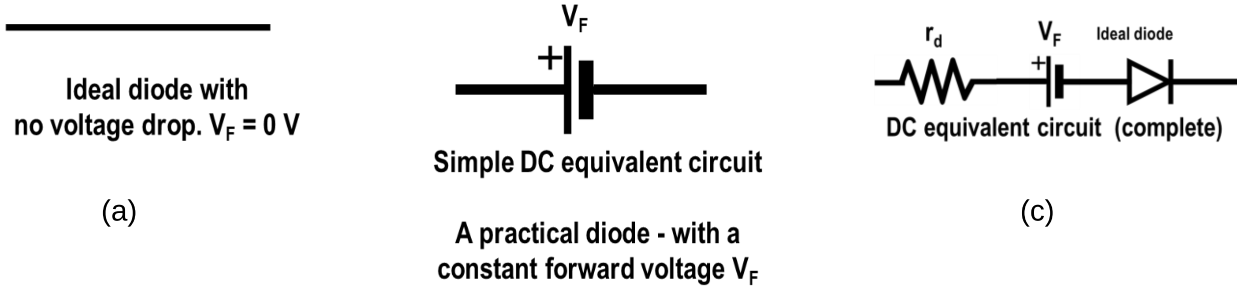
DC equivalent circuit (simple)

Fig 2.11

What is an equivalent circuit?
The electrical behaviour of the given circuit is accurately modelled using a combination of, simple electrical components such as Resistor (R), Inductor (L) and Capacitor (C).

Why equivalent circuit?
Equivalent circuit simplifies analysis of a complex circuit.

Some equivalent circuits of diodes are shown in fig 2.11 and 2.12. Eqvt circuit of an ideal diode is shown in Fig 2.12 (a) . In fig 2.12 (b) a practical diode with specific voltage drop V_F =0.7 V (Si) or 0.3 V (Ge) is shown. Has a constant V_F and negligible DC resistance (Zero)



(b)

Fig 2.12 Diode Equivalent circuits

In fig 2.11(c), a more complete equivalent circuit, with a specific V_F and a specific r_d is shown. r_d represents the ΔV_F part.

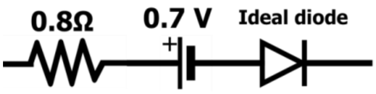


Fig 2.13

Problem 2.6: For the fig 2.13, what will be the drop across the silicon diode, if I_F = I0 mA and dynamic resistance is 0.8 Ω.

Ideal diode. $\therefore V_F$ = 0.7 V (Silicon, by default), I_F = 10 mA (given)

Drop across r_d = $I_F \times r_d$ = 10 mA X 0.8 Ω = 8 mV.

$\therefore$ Total drop across the diode = 0.7 V + 8 mV. = 0.708 V.

Problem 2.7: In the circuit shown in fig 2.14, calculate I_F . **(Unless otherwise mentioned, the diode is silicon by default.**

E = $I_F.R + V_F$

10 V = (I_F X 2.2K) + 0.7 V

$$\therefore I_F = \frac{10\ \text{V} - 0.7\ \text{V}}{2.2\ \text{K}} = 4.22\ \text{mA}.$$

Problem 2.8: For the same circuit in fig 2.14, what is the new I_F if the diode has a dynamic resistance of 0.3 Ω and R = 5 Ω .
The circuit is redrawn in fig 2.15.

$$E = I_F.R + I_F.r_d + V_F$$

10 V = (I_F X 5 Ω) + (I_F X 0.3 Ω) + 0.7 V

$$I_F = \frac{E - V_F}{R + r_d} = \frac{10\text{ V} - 0.7\text{ V}}{5\ \Omega + 0.3\ \Omega} = 9.3\text{ V} / 5.3\ \Omega = 1.76\text{ A}$$

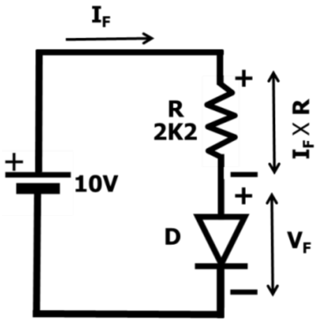


Fig 2.14

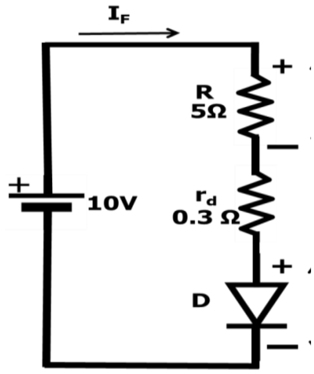


Fig 2.15

2.4 D C load line analysis (Diodes)

This topic mainly revolves around three subtopics

a) DC Load line

b) Diode V-I Characteristics

c) Q point.

2.4.1 How to draw a DC Load line? Refer fig 2.16

As per Kirchoff's Law, $\mathbf{E - (I_F \times R_L) - V_F = 0}$

$$E - V_F = I_F \times R_L$$

$$\frac{E}{R_L} - \frac{V_F}{R_L} = I_F$$

$$\therefore I_F = V_F\left(\frac{-1}{R_L}\right) + \frac{E}{R_L}$$

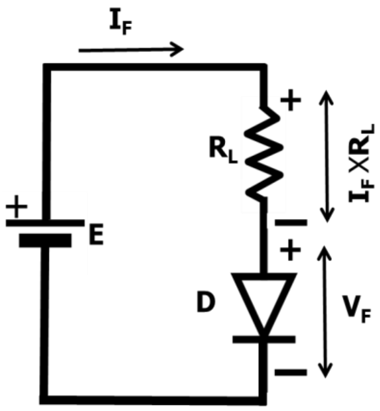


Fig 2.16

$\frac{E}{R_L}$ for a given circuit, is a constant.(say C)

$$\therefore I_F = V_F\left(\frac{-1}{R_L}\right) + C$$

This is of the form y = mx + c (Straight line equation).where slope $\mathbf{m = -\frac{1}{R_L}}$

The variables are the **DC conditions, I_F and V_F. Hence the name, DC load line.**

Problem 2.9: Let us draw a DC load line for the ckt in fig 2.16 where E = 6 V and R_L= 150 Ω

$$\mathbf{E = (I_F \times R_L) + V_F}$$

6 V = 150 I_F + V_F

(A) If I_F = 0, Then V_F = 6 V. For a diode, V_F = 6 V is of course absurd but a DC load line does not take the device characteristics into account

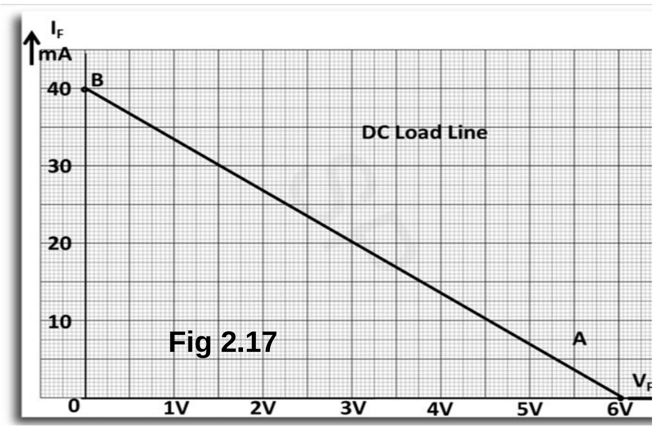


Fig 2.17

∴ **Point A = (6 V, 0 mA)**

(B) If V_F = 0, Then I_F $= \frac{6V}{150\ \Omega}$ = 40 mA.

∴**Point B =(0 V, 40 mA)**

Draw a graph using the above values.

- A has coordinates V_F = 6 V , I_F = 0 mA.
- B has coordinates V_F = 0 V , I_F = 40 mA.
- Join AB as a Straight line.
- This is the load line.
- Note, slope of this load line = **m =** $-\frac{1}{R_L}$

2.4.2 Diode VI characteristics

This is the same curve in fig 2.5 and 2.6. Diode VI characteristic is the forward bias region (first quadrant). This curve is super- imposed on the D C load line drawn above.

2.4.3 Q point (Quiescent point, DC bias point) – Refer fig 2.18

This is the point of intersection of DC load line and the diode V-I characteristics.

Problem 2.10: The Q point is (0.7 V , 35.3 mA). How?
For a silicon diode, V_F = 0.7 V.
Recall from fig 2.16,

$$6\ V = 150\ I_F + V_F$$
$$6\ V = 150\ I_F + 0.7\ V$$
$$5.3\ V = 150\ I_F$$
$$I_F = 35.3\ mA$$

∴ **Q point is (0.7 V , 35.3 mA).**

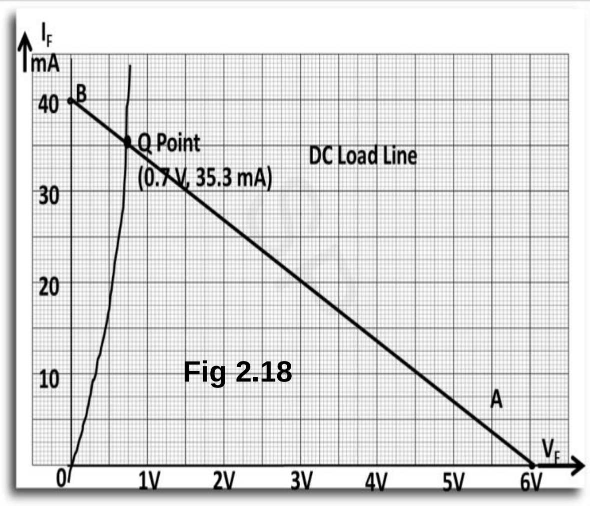


Fig 2.18

For the given circuit this Q point is fixed
Conclusion:
(1) For a given V_F and I_F, the Q point is unique.
(2) V_F for diodes is generally constant (0.7 V for Si and 0.3V for Ge)
(3) Therefore, for altering the Q point I_F should be changed
(4) I_F can be changed by either changing Input voltage E or R_L

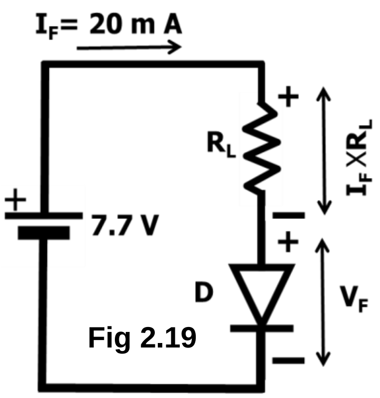


Fig 2.19

Problem 2.11: Find the load resistance for this circuit in fig 2.19, for $I_F = 20$ mA

1) Draw Load line

$V_F = E - I_F R_L$

a) For $I_F = 0$, $V_F = E = 7.7$ V.

∴ **Plot A at (7.7 V , 0 mA)**

b) Next, plot Q (Inter-section of diode characteristics and $I_F = 20$ mA line)

c) Join AQ and extend it to B. You will find B intersecting Y axis at $I_F = 22$ mA

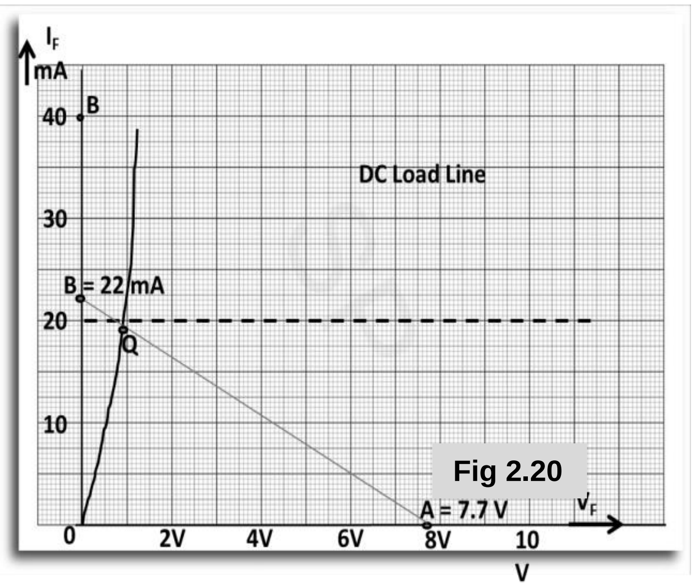


Fig 2.20

Why? Let us find I_F through circuit analysis

Problem 2.12: What is R_L from the load line?

We know that $V_F = E - I_F R_L$

ΔV_F = 7.7 V - 0.7 V = 7.0 V.

ΔI_F = 20 mA – 0 mA = 20 mA.

$$R_L = \frac{\Delta V_F}{\Delta I_F} = \frac{7V}{20\text{ mA}} = 350 \text{ ohms}$$

Using the equation **$V_F = E - I_F R_L$**

When $V_F = 0$, $E = I_F R_L$

$7.7\text{ V} = I_F \times 350\ \Omega$

$\therefore I_F = 7.7\text{ V} / 350\ \Omega = 22$ mA.

What is cut-in voltage or knee voltage of a diode?

The forward voltage at which the current through the junction starts increasing rapidly, is known as the **knee voltage or cut-in voltage**.

Typical cut-in voltages for values for Silicon diode is 0.7V and for Germanium diode is 0.3V.

Temperature effect on cut-in voltage:

Cut-in voltage decreases as temperature increases. Therefore didoe's forward voltage drop decreases as temperature increases.

Theoretical drop values are - 2.3 mV/ ^oC for silicon and - 2.12 mV/ ^oC for germanium. Can be approximated to – 2 mV/ ^oC.

2.4.4 Diode Parameters

1. I_F (max) - Maximum forward DC current permissible
2. V_F - Forward voltage drop (0.7 V for Si and 0.3 V for Ge)
3. V_{BR} - Maximum reverse voltage that can be applied, beyond which break down occurs

4. r_d - Dynamic resistance
5. I_R - Reverse saturation current (current flow when diode is reverse biased)
6. **Cut-in voltage or Knee voltage** - that forward voltage beyond which, forward current increases exponentially
7. P - continuous maximum power dissipation permissible at 25 deg C

2.4.5 Diode Capacitances

A p-n junction diode, will have two types of capacitance viz Transition capacitance (C_T) and Diffusion capacitance (C_D).

What is a capacitor?

- Capacitors store electric charge in the form of electric field.
- Charge is stored by using an arrangement of two electrically conducting plates (or electrodes) placed close to each other, separated by an insulating material called dielectric.
- The electrodes of the capacitor are good conductors and current can flow through them.

- But dielectric material is an insulator and current cannot flow through it. However, it efficiently allows electric field.
- When a voltage is applied to the capacitor, charge carriers flow through the conducting wire. but hits a roadblock from the dielectric or insulating material.
- Therefore, a large number of charge carriers get trapped at the electrodes of the capacitor and end up storing their electric charge.

- These charges in turn, exert an electric field between (across) the plates.
- The ability of the material to store electric charge is called capacitance.
- In a basic capacitor, the capacitance is directly proportional to the size of electrodes or plates and inversely proportional to the distance between two plates.

2.4.6 Transition capacitance

Now look at a diode

A reverse biased p-n junction diode is a typical capacitor. It stores electric charge at the **depletion region,** thanks to immobile positive and negative ions and the Depletion Region, therefore, acts like a dielectric in a capacitor.

The p-type and n-type regions have low resistance and act like electrodes (conducting plate) in a capacitor. Thus, p-n junction diode can be considered as a parallel plate capacitor.

Thus, there exists a capacitance at the depletion region.

When reverse bias voltage applied to the p-n junction diode is increased, we know, the width of depletion region increases and therefore, the capacitance of the reverse bias p-n junction diode decreases whenever reverse bias voltage increases.

The change of capacitance with changes in the reverse bias voltage is called transition capacitance (or depletion region capacitance or junction capacitance or barrier capacitance).

Transition capacitance can be defined as the change in electric charge (dQ) per change in voltage (dV).

$C_T = dQ / dV$

The transition capacitance is also given by,

$CT = \varepsilon A / W$

Where ε = Permittivity of the semiconductor, A = Area of plates or p-type and n-type regions and W = Width of depletion region

2.4.7 Diffusion capacitance or storage Capacitance - (C_D)

Diffusion capacitance occurs in a forward biased p-n junction diode.
In a forward biased diode, diffusion capacitance is quite large and transition capacitance is negligible
.
As we know, when forward bias voltage is applied to the p-n junction diode, recombination occurs in both sides of the junction and the width of depletion region decreases.

A large number of minority charge carriers, crowd around on either side of the depletion region hoping to recombine, with the majority carriers. As a result, a large amount of charge is stored at both sides of the depletion region, largely consisting of **minority electrons and minority holes.**

Thus the accumulation of holes in the n-region and electrons in the p-region is separated by a very thin depletion region or depletion layer. This depletion region acts like dielectric or insulator of the capacitor and charge stored at both sides of the depletion layer acts like conducting plates of the capacitor.

Diffusion capacitance is directly proportional to the electric current or applied voltage. Larger the electric current, larger the charge and larger the diffusion capacitance.

When the width of depletion region decreases, the diffusion capacitance increases. The diffusion capacitance value will be in the range of nano farads (nF) to micro farads (μF).

The formula for diffusion capacitance is

$C_D = \tau I_D / \eta V_T$, where τ is the mean life time of the charge carrier, I_D is the diode current and V_T is the applied forward voltage, and η is generation recombination factor. Diodes with high C_D, C_T values are **NOT SUITABLE for switching applications.**

2.5 Rectifiers

Define ''Rectifier''

Rectifier is a device such as diode, **that converts alternating current to direct current (ac to dc)**.

How is diode rectification done?

The rectification is done, by converting ac current to dc current, by suppression or inversion of alternate half cycles of the input.

2.5.1 Half wave rectifier (HWR):

Look at figure 2.21. A simple half wave rectifier is shown.

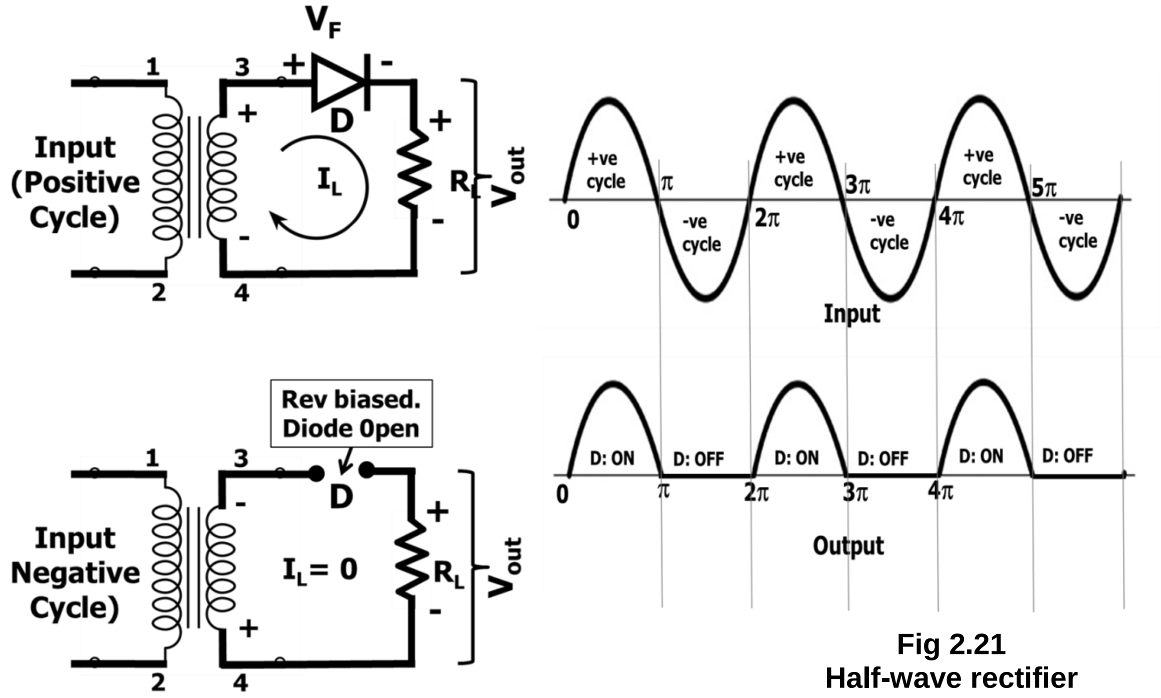


Fig 2.21
Half-wave rectifier

HWR Operation

Refer fig 2.21

- The input is fed through a transformer primary (terminals 1 and 2.).
- During +ve cycle of input, terminal 3 is +ve and terminal 4 is –ve.
- Diode gets forward biased and the current flow is clock wise, as shown in fig.
- Output voltage is I_L R_L.
- During – ve cycle of input # 4 is +ve and # 3 is –ve. Diode is reverse biased and diode behaves like an open circuit, as shown. No current flows in the circuit.
- The output voltage is zero. The peak inverse voltage across diode is, the input voltage (peak value).
- The Wave forms are shown in fig 2.21

Problem 2.13: For the circuit shown, determine the peak output voltage, peak load current and diode peak inverse voltage. The ac input is 10V, the load resistance is 1 kΩ and the diode is germanium.

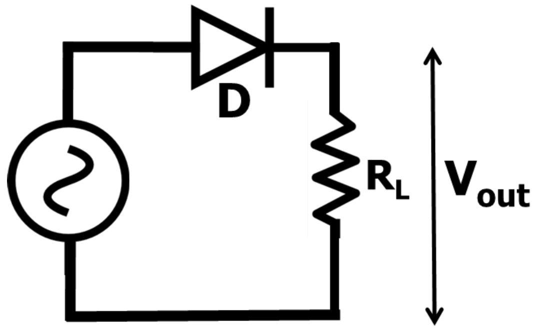


Fig 2.22

Important : Unless otherwise mentioned, the input is always specified as rms.

The relation between peak value & rms value is $V_{rms} = V_{peak} / \sqrt{2}$ and $I_{rms} = I_{peak} / \sqrt{2}$ and so on.

Input voltage is 10 V rms.

Input peak voltage: $V_{p\ in}$ = $\sqrt{2}$ X 10 V = 14.14 V

Output peak voltage: $V_{p\ out}$ = $V_{p\ in}$ - V_F

= 14.14 - 0.3 V = 13.84 V.

Peak load current = 13.84 V / 1 KΩ = 13.84 mA.

Peak inverse voltage = PIV = $V_{p\ in}$ =14.14 V.

2.5.2 Full wave rectifier (FWR):

-
- As the name implies **rectification happens, for both +ve and –ve cycles of the input** wave. Full wave rectifier, therefore, **uses 2 diodes.**
- A transformer input full wave rectifier (FWR) is shown in fig 2.23. The transformer becomes complex, with a centre-tap operation.

FWR Center tap transformer:

Look at fig 2.23.

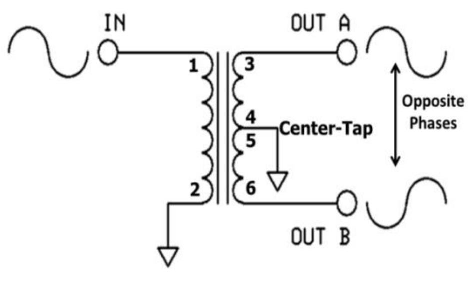


Fig 2.23 Center-tap transformer

It consists of a primary winding (1,2) and two secondary windings (3,4 and 5,6)

One end of, each of these secondary windings, is joined together. **In the figure 4 and 5 are joined.**

The windings normally have the same number of turns and therefore the 4, 5 junction becomes truly **a center tap.**

The sense of these two secondary windings is in such a way, that the **two secondary outputs always oppose each other, in phase.**

FWR Operation:

A full wave rectifier using two diodes is shown in fig 2.24.

NOTE center tap is at ground (0V) potential.

Note, diode cathodes are returned to ground through the load resistor R_L

Input: + ve half cycle (Refer fig 2.25)

- Terminal 3 is +ve, with respect to ground (center tap) and D1 is forward biased.
- Terminal 6 is –ve, with respect to ground (center tap) and D2 is reverse biased.
- Current flows in the Dl loop as shown. (**I_{L1}**)
- Resultant output **($V_{out\ 1}$)** is a +ve half cycle (Same phase as input).

Input: - ve half cycle (Refer fig 2.26)

- Terminal 6 is +ve, with respect to ground (center tap) and D2 is forward biased.
- Terminal 3 is –ve, with respect to ground (center tap) and D1 is reverse biased.
- Current flows in the D2 loop as shown. (**I_{L2}**)
- Resultant output **($V_{out\ 2}$)** is a +ve half cycle (Inverted with respect to input).
- The load current flows through R_L in the same direction (right to left) whether the input is a +ve half cycle or –ve half cycle. The load current is, the sum of the individual diode currents.
- Waveforms are shown in fig 2.27.

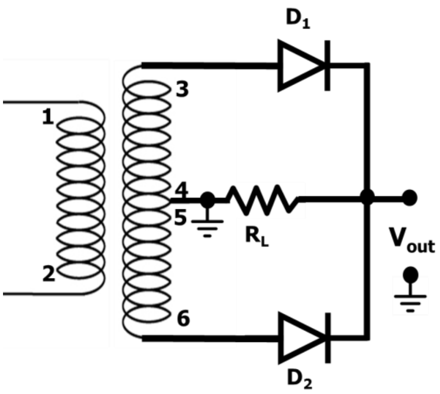


Fig 2.24 Full-wave rectifier Circuit (Two diodes)

2.5.2.3 Transformer related parameters

Let input voltage be $V_p = V_{pm}\ \sin wt$.

Let $\quad wt \quad = \alpha$

$\therefore V_p \quad = V_{pm}\ \sin \alpha$ (primary)

$V_s \quad = V_{sm} \sin \alpha$.

If the transformer has a turns ratio

N_p : N_s, then $\frac{N_S}{N_P} = \frac{V_{sm}}{V_{pm}}$

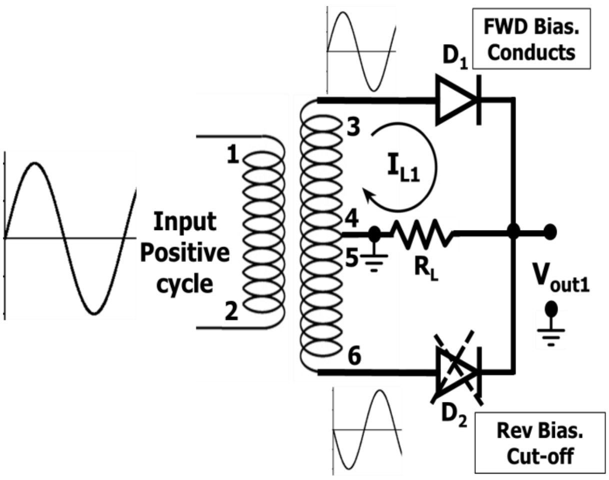


Fig 2.25 Full-wave rectifier operation

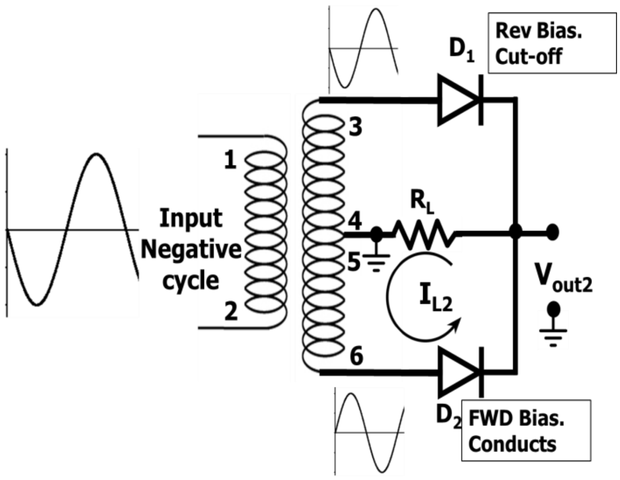


Fig 2.26 Full-wave rectifier operation

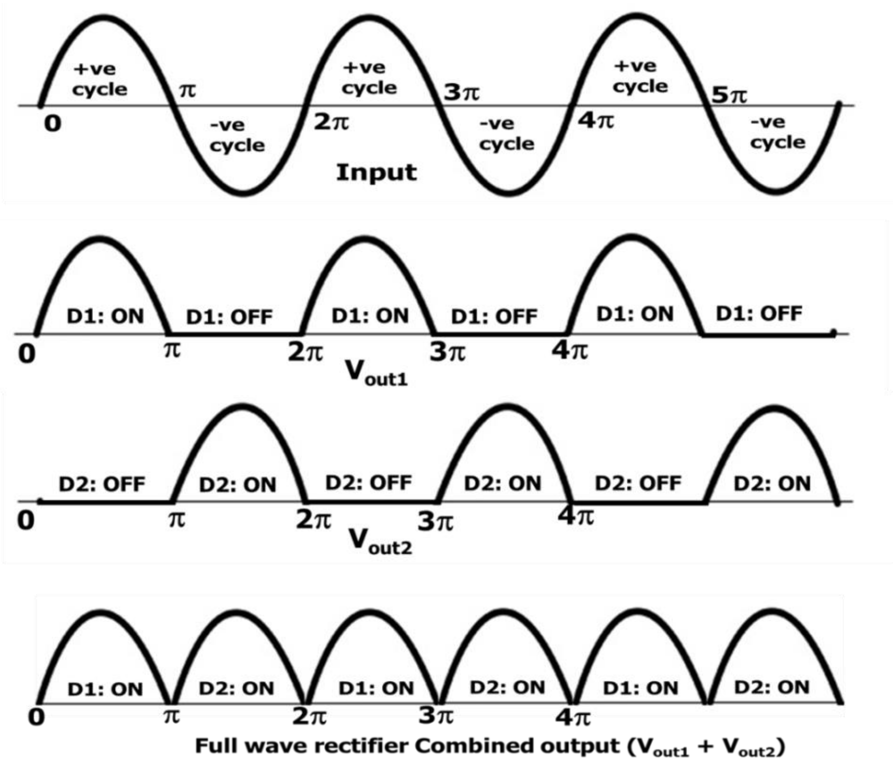


Fig 2.27 Full-wave rectifier waveforms

Transformer secondary resistance: The winding resistance R_s of transformer secondary, often comes into play, during current power calculations. .

Problem 2.14: What is the peak secondary current in this circuit in fig 2.28? Assume secondary has a resistance of 5 ohms.

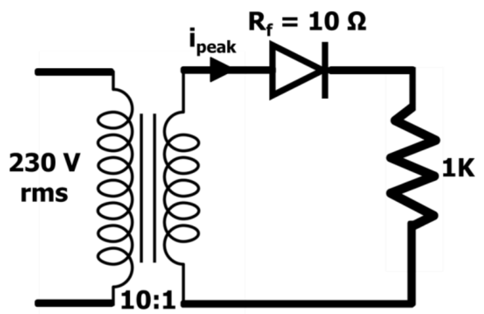


Fig 2.28

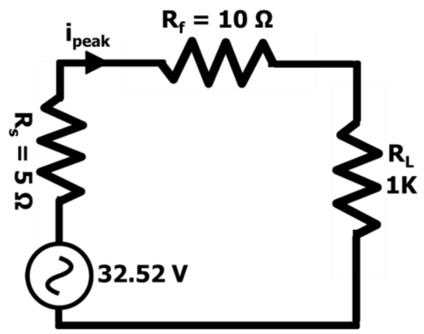


Fig 2.29

Secondary peak voltage = 32.52 V. (proceed as per previous example) . Refer equivalent circuit in fig 2.29.

Look at secondary equivalent circuit $\mathbf{i_m} = \frac{\mathbf{V_S}}{\mathbf{R_S+R_f+R_L}}$

i_{peak} (secondary) $= \frac{32.52\ \text{V}}{5\Omega + 10\Omega + 1000\Omega}$

= 32 .52 V / 1015 ohms = 32.04mA

-

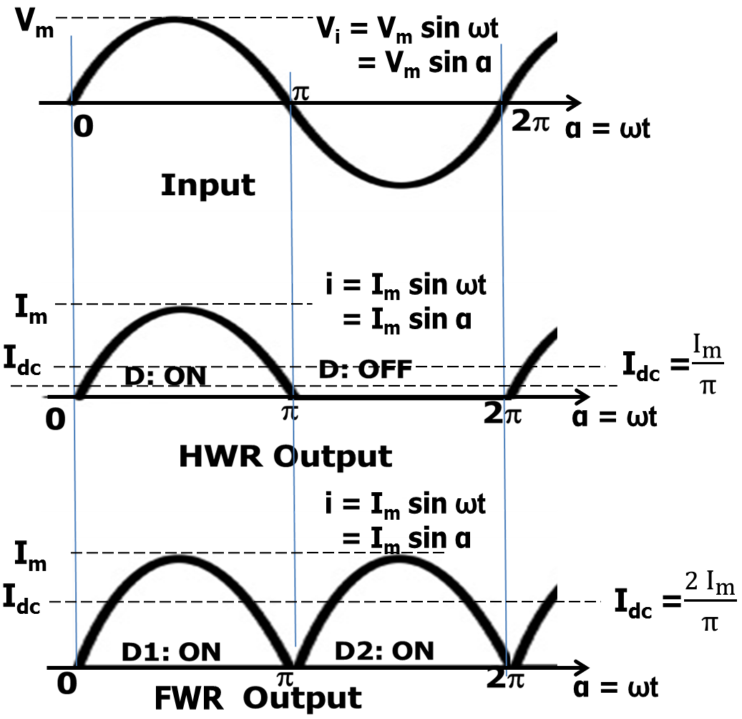


Fig 2.30 Rectifier equations

2.5.3 RECTIFIERS EQUATIONS (Refer fig 2.30)

Half wave	Full wave
<u>DC Current</u> I_{dc} $I_{dc} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\alpha\, d\alpha$ $= \frac{I_m}{2\pi}[-\cos\alpha]_0^{\pi}$ $= \frac{-I_m}{2\pi}[-1-1]$ $I_{dc} = \frac{I_m}{\pi}$ $I_{dc} = \frac{V_m}{\pi\,(R_f + R_L + R_S)}$	<u>DC Current</u> I_{dc} $I_{dc} = \frac{1}{\pi}\int_0^{\pi} I_m \sin\alpha\, d\alpha$ $= \frac{I_m}{\pi}[-\cos\alpha]_0^{\pi}$ $= \frac{-I_m}{\pi}[-1-1]$ $I_{dc} = \frac{2I_m}{\pi}$ $I_{dc} = \frac{2V_m}{\pi\,(R_f + R_L + R_S)}$
<u>DC output Voltage</u> V_{dc} $V_{dc} = I_{dc}R_L = \frac{I_M}{\pi}R_L$ $= \frac{V_M}{\pi\left(1+\frac{R_f}{R_L}\right)}$ (Assume $R_S = 0$)	<u>DC output Voltage</u> V_{dc} $V_{dc} = I_{dc}R_L = \frac{2I_M}{\pi}R_L$ $= \frac{2V_M}{\pi\left(1+\frac{R_f}{R_L}\right)}$ (Assume $R_S = 0$)

RMS current I $I = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d\alpha}$ $I = \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m{}^2 \sin^2\alpha\, d\alpha} \quad I = \frac{I_m}{2}$	RMS current I $I = \sqrt{\frac{1}{\pi}\int_0^{\pi} i^2 d\alpha}$ $I = \sqrt{\frac{1}{\pi}\int_0^{\pi} I_m{}^2 \sin^2\alpha\, d\alpha} \quad I = \frac{I_M}{\sqrt{2}}$
RMS output voltage across load $V_{rms} = I \times R_L = \frac{I_m}{2} \times R_L$ $V_{out} = \frac{V_M}{2\left(1+\frac{R_f}{R_L}\right)}$	RMS output voltage across load $V_{rms} = I \times R_L = \frac{I_M}{\sqrt{2}} \times R_L$ $V_{out} = \frac{V_M}{\sqrt{2}\left(1+\frac{R_f}{R_L}\right)}$
DC Output Power $P_{dc} = I_{dc}{}^2 R_L = \frac{I_m{}^2 R_L}{\pi^2}$ $= \frac{V_m{}^2 R_L}{\pi^2 (R_L + R_f)^2}$	DC Output Power $P_{dc} = I_{dc}{}^2 R_L = \frac{4 I_m{}^2 R_L}{\pi^2}$ $= \frac{4 V_m{}^2 R_L}{\pi^2 (R_L + R_f)^2}$
Total AC Input Power $P_{Diode} = I^2 R_f = \frac{I_m{}^2}{4} R_f$ $P_{RL} = I^2 R_L = \frac{I_m{}^2}{4} R_L$ $P_{in} = P_{Diode} + P_{R_L}$ $= \frac{I_m{}^2}{4}(R_f + R_L)$	Total AC Input Power $P_{Diode} = I^2 R_f = \frac{I_m{}^2}{2} R_f$ $P_{RL} = I^2 R_L = \frac{I_m{}^2}{2} R_L$ $P_{in} = P_{Diode} + P_{R_L}$ $= \frac{I_m{}^2}{2}(R_f + R_L)$
Rectifier efficiency $N = \frac{P_{dc}}{P_{in}} = \frac{\left(\frac{I_m{}^2}{\pi^2} \times R_L\right)}{\left[\frac{I_m{}^2}{4}(R_f + R_L)\right]}$ $= \frac{4}{\pi^2} \frac{R_L}{R_f + R_L}$ $= \frac{0.406}{1 + \left(R_f / R_L\right)}$ $= \frac{40.6}{1 + \left(R_f / R_L\right)}$	Rectifier efficiency $N = \frac{P_{dc}}{P_{in}} = \frac{\left(\frac{4 I_m{}^2 R_L}{\pi^2}\right)}{\left[\frac{I_m{}^2}{2}(R_f + R_L)\right]}$ $= \frac{8}{\pi^2} \frac{R_L}{R_f + R_L}$ $= \frac{0.812}{1 + \left(R_f / R_L\right)}$ $= \frac{81.2}{1 + \left(R_f / R_L\right)}$
Ripple Factor $r = \frac{I_{ac}}{I_{dc}}$ Please Note $I^2 = I_{dc}{}^2 + I_{ac}{}^2$ $\therefore \; r = \frac{\sqrt{I^2 - I_{ac}{}^2}}{I_{dc}} = \sqrt{\left(\frac{I}{I_{dc}}\right)^2 - 1}$	Ripple Factor $r = \frac{I_{ac}}{I_{dc}}$ $= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$

Form Factor is defined as $F = \frac{I}{I_{dc}}$ $F = \frac{\left(I_M/2\right)}{\left(I_M/\pi\right)} = \frac{\pi}{2} = 1.57$ Hence Ripple Factor $r = \sqrt{F^2 - 1}$ $r = \sqrt{1.57^2 - 1}$ $r = 1.21$	Form Factor is defined as $F = \frac{I}{I_{dc}}$ $F = \frac{I}{I_{dc}} = \frac{\left(I_M/\sqrt{2}\right)}{\left(2I_M/\pi\right)} = 1.11$ Hence Ripple Factor $r = \sqrt{F^2 - 1}$ $r = \sqrt{1.11^2 - 1}$ $r = 0.48$

Transformer utilization factor (TUF)
What is transformer utilization factor?

$$\mathrm{TUF} = \frac{\text{DC Power delivered to load}}{\text{AC Power rating of transformer}}$$

Half wave Rectifier

$$P_{DC} = {I_{DC}}^2 \times R_L = \left(\frac{I_m}{\pi}\right)^2 \times R_L$$

$$P_{ac}(rms) = V_{rms} \times I_{rms}$$

$$P_{ac}(rms) = \frac{V_M}{\sqrt{2}} \times \frac{I_M}{2}$$

$$I_m = \frac{V_M}{R_S + R_f + R_L}$$

But $V_m = I_m R_L$

$$\therefore \ \mathrm{TUF} = \left(\frac{{I_m}^2 R_L}{\pi^2}\right) \Big/ \left(\frac{{I_m}^2 R_L}{2\sqrt{2}}\right)$$

$$= {2\sqrt{2}}/{\pi^2} \quad = 0.287$$

Full wave Rectifier

$$P_{DC} = {I_{DC}}^2 \times R_L = \left(\frac{2I_m}{\pi}\right)^2 \times R_L$$

$$P_{ac}(rms) = V_{rms} \times I_{rms}$$

$$P_{ac}(rms) = \frac{V_M}{\sqrt{2}} \times \frac{I_M}{\sqrt{2}}$$

But $V_m = I_m \times R_L$

$$\therefore \ \mathrm{TUF} = \frac{\left(\frac{4}{\pi^2} \times {I_m}^2 R_L\right)}{\left(\frac{{I_m}^2 R_L}{2}\right)}$$

$$= \frac{8}{\pi^2} \quad = 0.812$$

Problem 2.15 : The input signal is 50v in amplitude with a frequency of 50 H_Z. Calculate

(a) Rectifier efficiency
(b) Ripple Factor

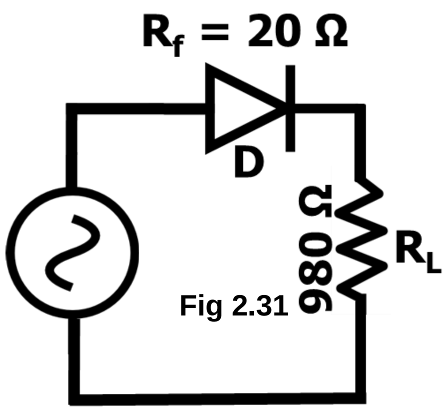


Fig 2.31

Refer fig 2.31, Before we find m, we need to find

(a) Peak, Average (DC) and rms values of load current
(b) DC power output
(c) AC Power input
(d) Note, there is no transformer, ∴ Rs = 0

(a) Peak load current = $I_m = \frac{V_m}{R_f+R_L+R_S} = \frac{50}{20+980\Omega}$ = 50mA

$I_{dc} = {}^{I_m}/_{\pi} = \frac{50}{3.14} = 15.92\text{mA} = 15.92 \times 10^{-3}\text{A}$

$I_{rms} = \frac{I_m}{2} = \frac{50}{2} = 25\text{mA} = 25 \times 10^{-3}\text{A}$

(b) $V_{DC} = I_{DC} \times R_L = 15.92 \times 10^{-3} \times 980\Omega = 15.6\text{ V}$

$P_{DC} = {I_{DC}}^2 \times R_L = 15.92^2 \times 980 = 248.4\text{ mW}$

(c) AC Power input = $(I_{rms})^2 \times (R_L + R_f)$
= $(25 \times 10^{-3})^2 \times (980 + 20)$
= 625 mw

(d) Rectifier efficiency = $\frac{P_{dc}}{P_{ac\ in}} = \frac{248.4\text{ mW}}{625\text{ mW}}$ = 39.74%

(e) Ripple factor = $\sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{25\text{ mA}}{15.92\text{ mA}}\right)^2 - 1}$ = 1.21

(f) % regulation = $\frac{V_{no\ load} - V_{full\ load}}{V_{load}}\text{ X } 100\%$

(g) $V_{no\ load}$ = V_{DC} = $\frac{V_m}{\pi} = \frac{50}{\pi}$ = 15.91 V

(h) V_{load} = V_{DC} = 15.6 V

(j) Therefore % regulation = $\frac{15.91-15.6}{15.6}$ = 1.98%

Problem 2.16: For the example 2.14, already solved, find
(a) Peak, average & rms load currents
(b) DC Power output & ac power input
(c) Efficiency
(d) Form factor
(e) Ripple Factor

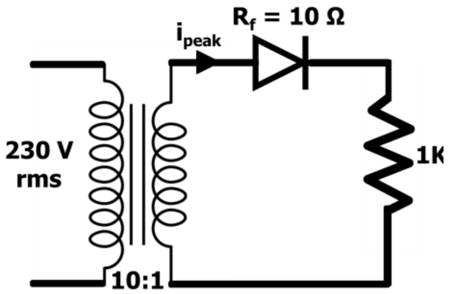


Fig 2.32

Refer fig 2.32. From 2.14, the peak secondary voltage V_m = 32.52 V

(a) Peak, average & rms load

$I_m = \frac{V_m}{R_S+R_f+R_L} = \frac{32.52}{5+10+1000} = \frac{32.52}{1015}$ = = 32.04mA

$I_{DC} = \frac{I_m}{\pi} = \frac{32.04\text{ mA}}{\pi} = 10.2\text{mA}$

$I_{rms} = \frac{I_m}{2} = \frac{32.04\text{ mA}}{2} = 16.02\text{mA}$

(b) DC Power output & ac power input

$V_{DC} = I_{DC} \times R_L = 10.2\text{ mA} \times 1000\,\Omega = 10.2\text{ V}$

$P_{DC} = (I_{DC})^2 \times R_L = (10.2\text{mA})^2 \times 1000\Omega = 104\text{ mW}$

$P_{ac\,in} = (I_{rms})^2 \times (R_S + R_f + R_L) = (16.02)^2 \times (5 + 10 + 1000) = 260.5\text{mW}$

(c) Efficiency $= \frac{P_{DC}}{P_{ac\,in}}\% = \frac{104\text{mW}}{260.5\text{mW}}\% = 39.92\%$

(d) Form factor $= \frac{I_{rms}}{I_{dc}} = \frac{16.02\text{mA}}{10.02\text{mA}} = 1.57$

(e) Ripple Factor $\gamma = \sqrt{F^2 - 1} = \sqrt{1.57^2 - 1} = 1.21$

Problem 2.17: The input to a full wave rectifier is 25 sin 100πt. The load resistor is 200Ω. Silicon diodes (0.6 V) with 50 Ω diode resistance is used. What is the peak output voltage, peak current and peak inverse voltage?

The diodes are silicon (0.6 V).

What is the frequency of the signal?

Input = 25 sin 100πt, Compare this with $V = V_m \sin \omega t$.

$\therefore V_m =$ 25V (peak) $\omega = 2\pi f t = 100\pi t$ $\therefore f = 50\text{Hz}$

Input voltage (peak) = 25 V

Output voltage (peak) = 25 V − V_F = 25 V − 0.6 V = 24.4 V

Output Current = 24.4V/(200Ω + 50Ω) = 97.6 mA

PIV = Peak inverse voltage is the voltage across the diode, during reverse bias conditions

PIV of FWR = $2V_M$= 2 X 25 V= 50 V

Problem 2,18: In a full wave rectifier the secondary of the transformer used is 30 – 0 – 30 V. The secondary resistance is 20Ω. The diodes have forward resistance of 20 Ω and load resistor of 170 Ω

(a) Calculate Peak, average and rms currents,

(b) Calculate DC output power, ac input power and efficiency

(c) Calculate form factor, ripple factor and % regulation.

The secondary of a FWR is from a center tapped transformer. Look at the figure 2.33

30V is the rms value (not peak value)

The diode is fed through one half of the secondary (0 – 30 V)

$\therefore$ RMS input for each diode $V_{rms} = 30\text{ V}$

$V_m = 30 \times \sqrt{2} = 42.42\text{ V}$

$$I_m = \frac{V_m}{R_S + R_f + R_L}$$

Secondary resistance given = 20 Ω (for full secondary)

R_S = 10 Ω for each half of the secondary.

$$I_M = \frac{42.42\text{ V}}{10\Omega+20\Omega+170\Omega} = \frac{42.42\text{V}}{200\Omega} = 212\text{mA}$$

$$I_{DC} = \frac{2I_M}{\pi} = \frac{2 \times 212\text{mA}}{\pi} = 134.9\text{mA}$$

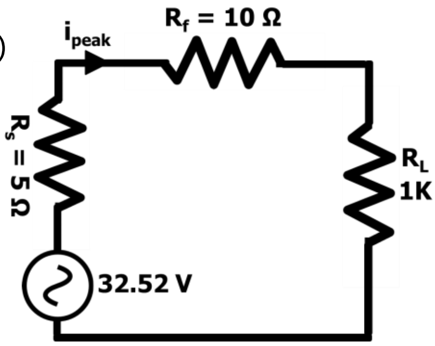


Fig 2.33 Equivalent Circuit

$$I_{rms} = \frac{I_M}{\sqrt{2}} = \frac{212\text{mA}}{\sqrt{2}} = 149.9\text{mA}$$
$$P_{DC} = {I_{DC}}^2 \times R_L = (134.9)^2 \times 170 = 3.1 \text{ W}$$
$$P_{ac\,in} = {I_{rms}}^2 \times (R_S + R_f + R_L) = (149.9)^2 \times (10 + 20 + 70) = 4.49 \text{ W}$$
$$\eta = \frac{P_{DC}}{P_{ac}}\% = \frac{3.1 \text{ W}}{4.49 \text{ W}} \times 100 = 69\%$$
Form Factor $= \frac{I_{rms}}{I_{DC}} = \frac{149.9}{134.9} = 1.11$

Ripple Factor $= \sqrt{(F)^2 - 1} = \sqrt{(1.11)^2 - 1} = 0.48$

% Regulation $= \frac{V_{NL} - V_{FL}}{V_{FL}}$

$$V_{DC}(\text{No Load}) = \frac{2V_M}{\pi} = \frac{2 \times 42.42}{\pi} = 27 \text{ V}$$
$$V_{FL} = I_{DC} \times R_L = 134.9 \times 170 = 22.9 \text{ V}$$
% Regulation $= \frac{27\text{V} - 22.9\text{V}}{27\text{V}} \times 100 = 15.2\ \%$

2.5.4 Bride rectifier (BR)

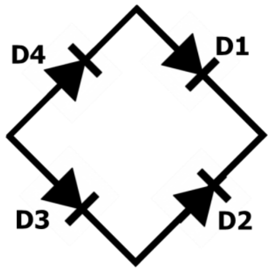


Fig 2.34. Bridge.

What is a bridge in a bridge rectifier?

A Basic bridge rectifier is shown in fig 2.34

It is an arrangement of **4 diodes** in such a way that

- full wave rectification happens
- **2 diodes conduct during the +ve** input cycle and the **other two diodes conduct during the -ve** input cycle.

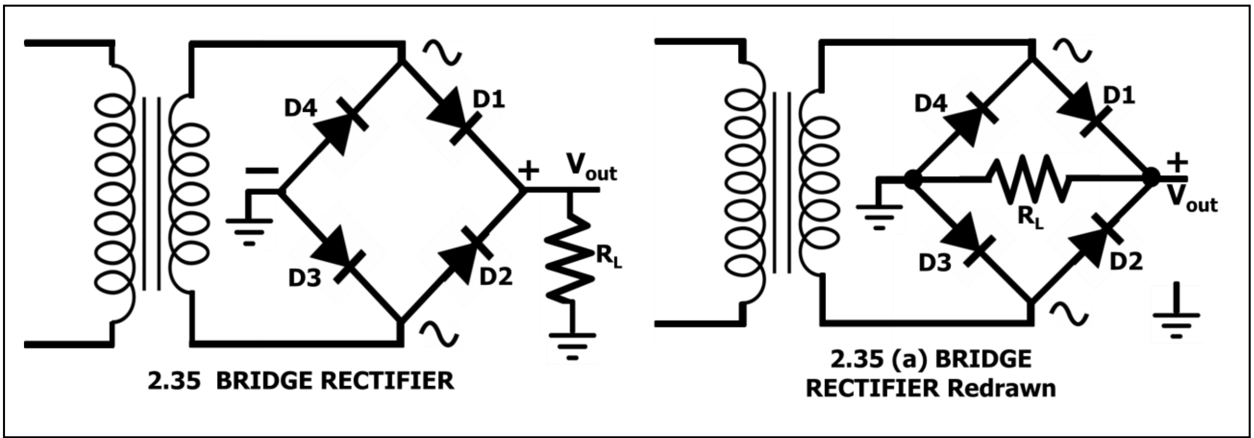
It is a full wave rectifier .

It consists of 4diodes

- It does not require a center tap secondary.
- Input is applied in the primary winding.

BR Operation:

A bridge rectifier is shown in fig 2.35



The same bridge rectifier is redrawn to provide more clarity in fig 2.35(a).

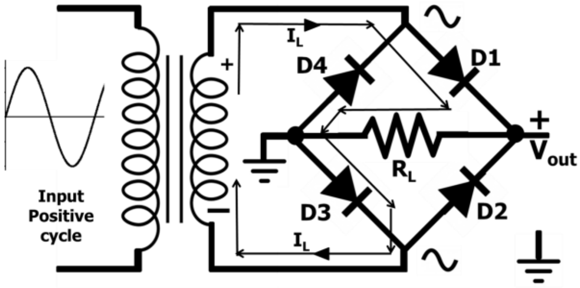


Fig 2.36 BRIDGE RECTIFIER (Redrawn)
Positive cycle (Only D1 and D3 conduct)

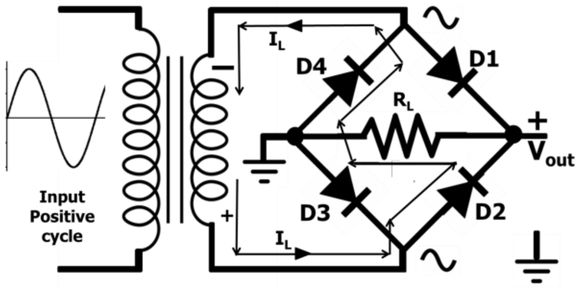


Fig 2.36 (a)BRIDGE RECTIFIER
Negative cycle (Only D2 and D4 conduct)

+ve cycle:

When the input is a +ve cycle, top of the secondary is +ve and the bottom is –ve.
Diodes D1 and D3 will conduct as shown in fig 2.36.

– ve Cycle:

When the input is a -ve cycle, bottom of secondary is +ve and the top is –ve.
Diodes D2 and D4 will conduct as shown in fig 2.36(a).
Note, the current through R_L**, is in the same direction (right to left)**, in both cycles

Equations of bridge rectifier:

They are same as that of FWR, except I_m

$$I_m = \frac{V_m}{R_s + R_f + R_f + R_L}$$ [since, 2 diodes are involved, per cycle]

$$I_{DC} = 2\,\frac{I_m}{\pi}, \qquad V_{DC} = 2\,\frac{V_m}{\pi}, \qquad I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$P_{DC} = (I_{DC})^2 \times R_L = \frac{4}{\pi^2} I_m^2 R_L$$

$$P_{ac} = I^2_{RMS}(R_S + 2R_f + R_L) = \frac{I_m^2}{2}[R_S + 2R_f + R_L]$$

$$\text{Efficiency } (\eta) = \frac{8}{\pi^2}[R_L / (R_S + 2R_f + R_L)]\,\% = 81.2\,\%$$

F = 1.11, ϒ = 0.48, TUF = 0.812

2.5.5 Comparison of rectifiers

Compare advantages & disadvantages of all the three rectifiers.

H W	F W	Bridge
Only one diode. Easy design.	2 diodes. Complex design.	4 diodes. Complex design.
No centre-tap transformer	Centre-tap transformer	No centre-tap transformer
Ripple factor high. (1.21)	Ripple factor Low. (0.48)	Ripple factor low. (0.48)
TUF low. Inefficient.	TUF High. Efficient.	TUF high. Efficient.

Low efficiency 40.6%.	High efficiency 81.2%.	High efficiency 81.2%.
Output load voltage & current low	Output load voltage & current high.	Output load voltage & current high.
Uni-directional current through transformer. Therefore transformer can saturate.	No net dc current through transformer. Therefore transformer will not saturate.	Current is continuous always hence transformer can be small & Inexpensive.
PIV of diode low (V_m)	PIV of diode high (2 V_m)	PIV of diode low (v_m)

Problem 2.19: In a bridge rectifier, the transformer primary voltage is 200 sin wt. The transformer step down ratio is 4 : 1. The secondary resistance is 10 ohms. Forward resistance of the diode is 20 ohms and the load resistance is 450 ohms.

Calculate I_m, I_{DC}, I_{rms}, V_{DC}, Ripple factor, Efficiency (η) and PIV of the diode.

V_p = 200 sin wt N1: N2 = 4 : 1 $\therefore V_s = \frac{200 \text{ Sin wt}}{4}$ = 50 sin wt V_m = 50 V.

$$I_m = \frac{V_m}{R_s + 2R_f + RL} = \frac{50\text{ V}}{10 + (2 \text{ X } 20) + 450} = 100 \text{ mA}$$

$$I_{DC} = \frac{2I_m}{\pi} = \frac{200}{\pi} = 63.6 \text{ mA}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} = \frac{100}{1.414} = 70.7 \text{ mA}$$

V_{DC} = I_{DC} X R_L = 63.6 X 450 = 28.6 V

P_{DC} = $(I_{DC})^2$ X R_L = $(63.6)^2$ X 450 = 1.82 W

P_{ac} = I_{rms}^2 X (R_s + 2 R_f + R_L) = $(70.7)^2$ X (10 + 40 + 450) = 2.49 W

Efficiency $= \frac{P_{DC}}{P_{ac}}\,\%$ $= \frac{1.82\text{ W}}{2.49\text{ W}}\,\%$ =73.09 %

Ripple factor $= \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$ $= \sqrt{\left(\frac{70.7}{63.6}\right)^2 - 1}$ = 0.4854

PIV for a bridge rectifier = V_m = 50 V

2.5.6 Rectifiers: Quick reference guide

Parameters	**HW**	**FW**	**BR**
Load current I_m	$\frac{V_m}{R_s + R_f + RL}$	$\frac{V_m}{R_s + R_f + RL}$	$\frac{V_m}{R_s + 2R_f + RL}$
I_{DC} – Average DC current	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
V_{DC} - Average DC voltage	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$

I_{rms}	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
V_{rms}	$\frac{V_m}{2}$	$\frac{V_m}{\sqrt{2}}$	$\frac{V_m}{\sqrt{2}}$
P_{DC} - DC Power output	$\left(\frac{I_m}{\pi}\right)^2$	$\left(\frac{2I_m}{\pi}\right)^2$	$\left(\frac{2I_m}{\pi}\right)^2$
P_{ac} - AC Power output	$\left(\frac{I_m}{2}\right)^2 (R_s + R_f + R_L)$	$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_s + R_f + R_L)$	$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_s + 2R_f + R_L)$
Efficiency	40.6%	81.2%	81.2%
Form factor	1.57	1.11	1.11
Ripple factor	1.21	0.482	0.482
TUF	0.287	0.812	0.693
Ripple freq	f	2f	2f
PIV	V_m	2 V_m	V_m

2.6 Capacitor Filter Circuit

2.6.1 Half-wave rectifier with Capacitor filter

Fig 2.37 shows a HW rectifier, with a capacitor filter. Let us assume an ideal diode . V_F =0

Operation

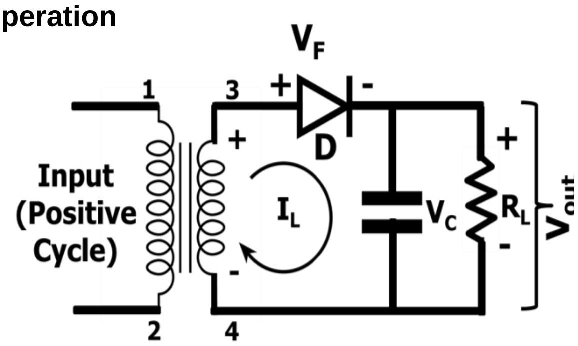


Fig 2.37 Capacitor Input filter

What happens in cycle 1? 0 to 90 deg (Refer fig 2.38)

- Input is switched on. During the first quarter positive cycle (0 to 90 deg) of the input, the diode conducts and the capacitor charges to the peak value of the input .

90 deg to 360 deg [Refer fig 2.38(a)]

- From 90 deg to 360 deg of the first cycle the *diode does not conduct .*

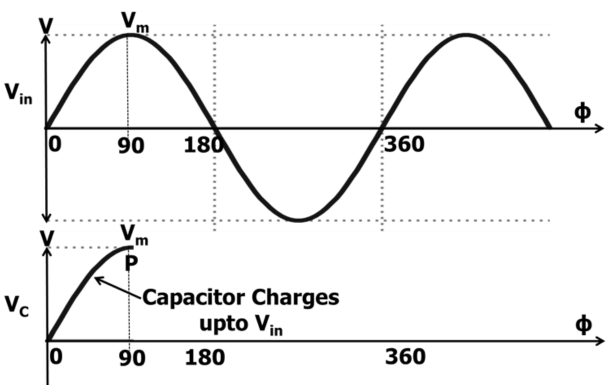


Fig 2.38 HWR Capacitor filter action (0 to 90 deg)

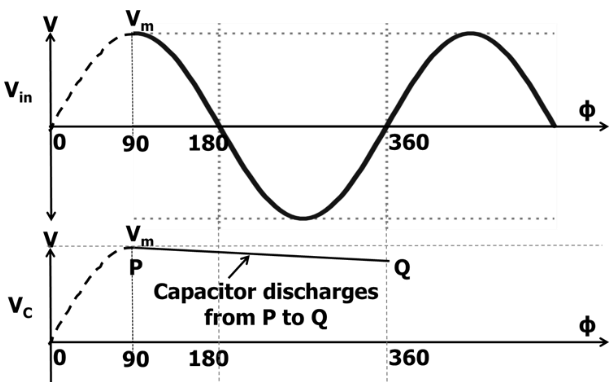


Fig 2.38 (a) HWR Capacitor filter action (90 to 360 deg)

Why ? (Refer fig 2.40 and 2.41)

- Let us say the sine wave has a peak voltage V_m =5 V. Up to P, the capacitor charges, simply following the input voltage. Therefore, the capacitor voltage will be 5V at P.

- The input voltage starts reducing beyond P (< 5 V). But the capacitor is already at 5V. Therefore, the diode finds itself getting reverse biased beyond P. (Cathode = 5 V and anode is , 5 V)

- Refer fig 2.39. The capacitor slowly discharges from its 5 V, through the resistor R_L The rate of discharge is determined by the time constant R_LC. Greater the time constant, slower will be the discharge.

What happens in Cycle 2? (Refer Diagram 2.39.)

- The capacitor is fully charged up to 5 V at P. The capacitor discharges in the rest of the cycle 1 and up to Q in cycle 2.
- Let us say, at Q the capacitor has discharged up to 4 V.
- The input also is at 4V at Q and rising. Look at interval QR. In this interval, the input (anode) will be more +ve than the capacitor (cathode). The diode gets forward biased in QR. Consequently the capacitor charges again by following the input. At R, the input is 5 V & the capacitor also is at 5 V.
- Beyond R, the input voltage will be less than that of capacitor. Diode is reverse biased. Capacitor starts its slow discharge. This cycle keeps repeating.

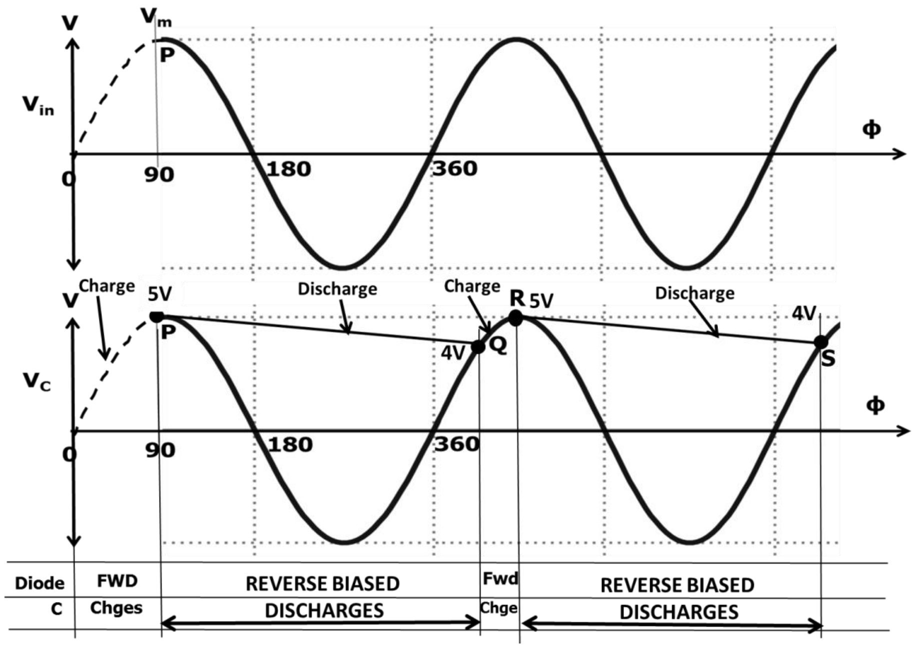


Fig 2.39 HWR Capacitor filter action (2 cycles)

Time constant

- The capacitor in HW rectifier, has two time constants, one for charging and one for discharging.
- Charging is through the diode whose resistance R_f is very low.
- Time constant is small and the capacitor charges very quickly. (Imagine filling up a bucket with a very large inlet tap).
- Discharging is through the resistor R_L whose value is relatively high.

- Time constant is large and the capacitor discharges very slowly. (Imagine emptying the bucket through a very small outlet tap).

Output ripple will be less as seen above. The ripple factor ϒ, frequency, capacitor value and the load resistor are inter-related by the equation,

- **For a half wave rectifier, ϒ =** $\frac{1}{2\sqrt{3}\,CfR_L}$

2.6.2 Full wave rectifier with capacitor filter

The theory is exactly similar to HW rectifier discussed earlier. The circuit diagram of FWR and the wave forms are shown in fig 2.40

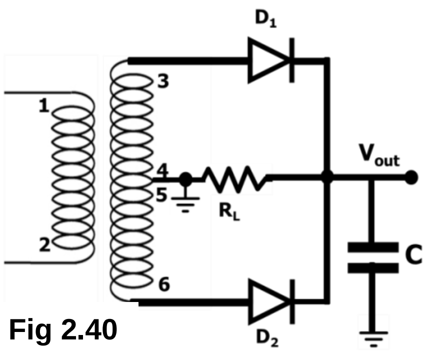
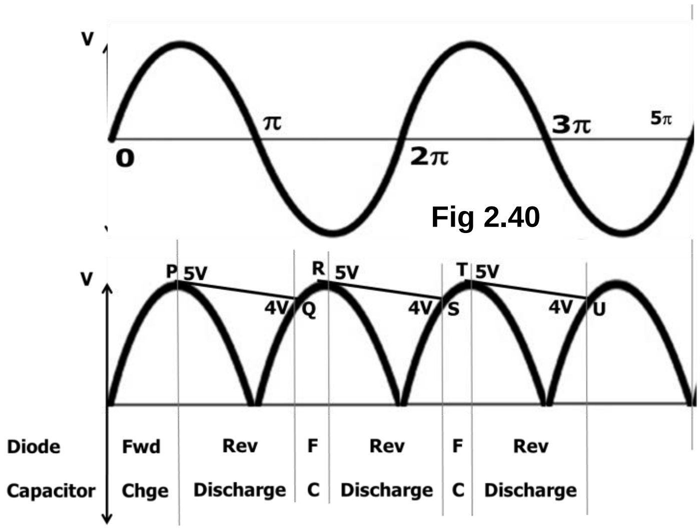


Fig 2.40

Full wave rectifier with Capacitor filter



Wave forms are shown in fig 2.40(a)

Why capacitor filter? **Fig 2.40(a) FWR - Capacitor filter action (2 cycles).**

Output ripple will be less as seen above. The ripple factor ϒ, frequency, capacitor value and the load resistor are inter-related by the equation,

For a full wave rectifier, ϒ = $\frac{1}{4\sqrt{3}\,CfR_L}$

Problem 2.20: If a full wave rectifier is fed a sine wave of 10 V, 400 Hz, what is the capacitor value required, if the load current required is 20 mA and ripple factor is 2 %

Full wave rectifier →.Ripple = 2f = 800 Hz.

What is R_L?

$V_{DC} = \frac{2V_m}{\pi}$

$I_{DC} \times R_L = \frac{2V_m}{\pi}$ $\quad\quad R_L = \frac{2V_m}{\pi} \times \frac{1}{I_{DC}}$

Sine wave i/p = 10 V (rms) [unless otherwise mentioned V is rms]

V_m = 10 V X $\sqrt{2}$ = 14.14 V

I_{DC} = 20 mA

$\therefore R_L \quad = \dfrac{2 \text{ X } 14.14}{20 \text{ X } 20 \text{ X } 10^{-3}} \quad = 450\ \Omega$

Ripple factor $\Upsilon \quad = \dfrac{1}{4\sqrt{3}\,CfR_L}$

$\dfrac{2}{100} \quad = \dfrac{1}{4X1.732X800X450} \quad = 2 \text{ X } 10^{-5} \quad$ = 20 micro farad (μF)

2.7 <u>Zener diode voltage regulator</u>

Refer fig 2.41

- Zener diode is a special type of diode.
- It is widely used as a **voltage reference** in DC regulated power supplies
- Zener is always used in the **reverse bias** conditions.
- When the reverse bias exceeds a specified value, reverse current (I_R) flows, almost **unlimited.**
- This voltage is called **break down voltage or Zener voltage or Knee voltage.**
- The Zener diode circuit Symbol is shown here.

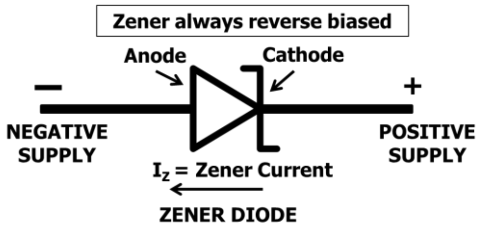


Fig 2.41 Zener Diode - Symbol , biasing and current flow

2.7.1 Zener characteristics

Fwd characteristics: The forward characteristics is same as that of a normal diode.

Rev characteristics (refer fig 2.42 and 2.43)

- The diode is operated in **reverse bias mode (Anode: – ve, Cathode: +ve).**
- Up to some reverse voltage, reverse current is low.
- Beyond a specific reverse voltage, the **pn junction breaks down**.
- This is known as **Zener break down.**
- Large **unlimited reverse current** flows.
- The zener **maintains a steady voltage over a large current range** as seen in figure.
- It is necessary to **limit the current** by using a series resister R1.
- The break down action is **reversible**. Zener diode can be used again and again.

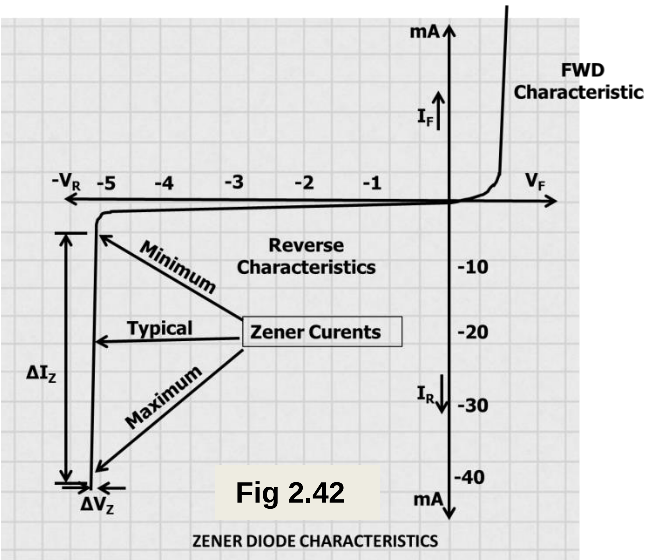


Fig 2.42 Zener Diode Characteristics

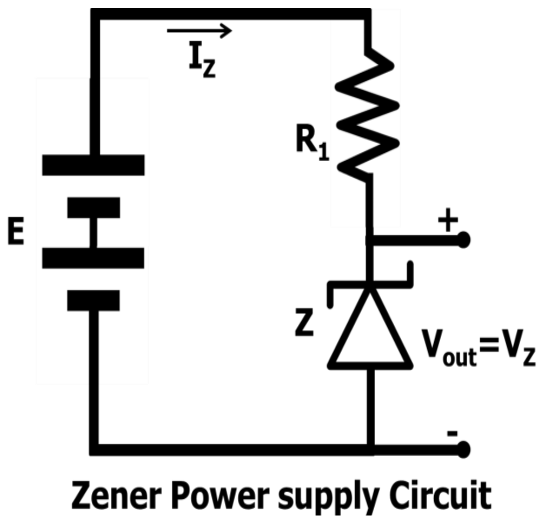


Fig 2.43

What is the zener current in this circuit without a load resistor? (fig 2.43)?

$$I_Z = \frac{E - V_Z}{R_1}$$

What is the zener current in the circuit in fig 2.44, with a load resistor R_L? What is the load current in this circuit?

$$I_Z + I_L = \frac{E - V_{out}}{R_1} = \frac{E - V_Z}{R_1}$$

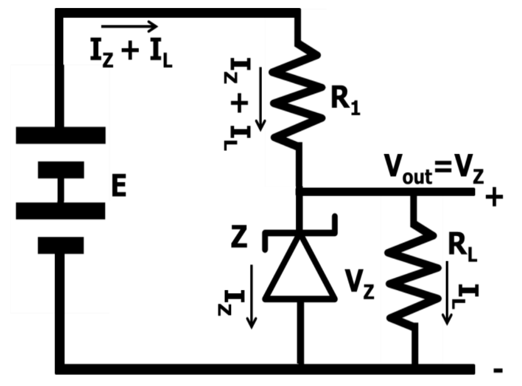
$$I_L = \frac{V_Z}{R_L}$$

2.7.2 Zener break down mechanism

<u>Case 1</u>

<u>Very narrow depletion region</u>

- **Reverse voltage produces very high field strength**.
- What is field strength? Voltage per distance **(Volts / Distance.)**
- **Electrons break away from their atoms due to this field strength**.
- ∴Due to this electron flow, depletion region is converted into a conductor (from insulator)
- This is called **ionization by electric field**
- This is one of the Zener break down mechanisms
- Usually occurs when **reverse bias is < 5V**



Zener Power supply with Load
(Curent Distributions)

Fig 2.44

<u>Case 2</u>

<u>Depletion region very wide</u>

- In the reverse bias mode reverse saturation current flows.
- There are electrons moving in reverse saturation current.
  - **When these electrons travel in the wide depletion region, these electrons gain a lot of energy**
  - These energetic electrons **collide with atoms** and cause their **electrons to break-free**.
  - Due to these new electrons, **more collisions** occur and more electrons get released
- This is known as **Avalanche break-down**.

2.7.3 Power dissipation of a Zener

What is maximum power dissipation P_D of a Zener?

The **Zener operates in a break down mode. (Reverse bias**).

Once break down happens, **current through the Zener is unlimited**.

This **current should be limited** through a resistor.

Otherwise Zener will dissipate too much power, get heated and **burn itself out**.

Power dissipated in the **Zener $P_D = V_Z \times I_Z$** (refer figure 2.44)

Every Zener has a specification for **Maximum power dissipation P_D max** and the designer should ensure that the Zener is **operated with in P_D max (by choosing E & R carefully)**

Problem 2.17: What should be value of R, in fig 2.45, if the Zener break down voltage is 8 V and P_D max = 400 mW

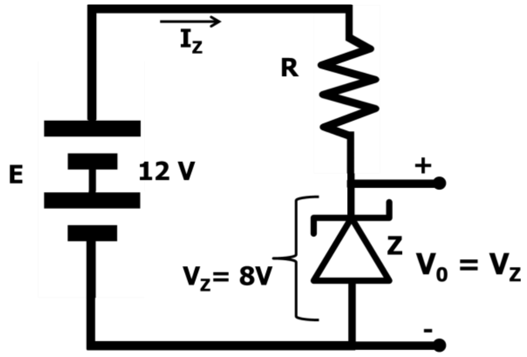


Fig 2.45

$P_D = V_Z \times I_Z$

$400\ mW = 8\ V \times I_Z$

$\therefore I_Z = 50\ mA$

The resistor must ensure I_Z is < 50 mA

Input voltage = 12 V

Zener voltage = 8 V

Voltage across resistor R = 4 V

Current through resistor R = 50 mA

$\therefore$Value of R $= \frac{4\ \mathbf{V}}{50\ \mathbf{mA}} = 80\ \Omega$

R = 80 Ω

Problem 2.18: V_Z =10V, R =500. For this circuit in fig 2.46, what is the current through the Zener?

What is P_D of Zener?

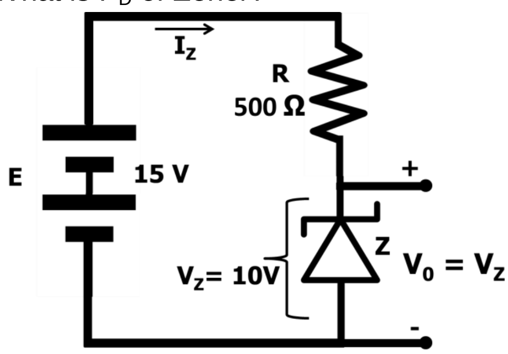


Fig 2.46

V_Z = 10 V. R = 500 Ω

$\therefore$ Voltage across resistor = 15 V – 10 V = 5 V

Current through R $= \frac{5\ V}{500\ \Omega}$ = 10 mA

Current thro Zener also = 10 mA

P_D of zener = $V_Z \times I_Z$ = 10 V X 10 mA = 100 mW.

2.7.4 Equivalent circuit of Zener

DC Equivalent circuit

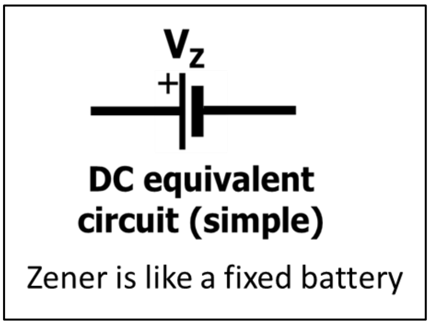
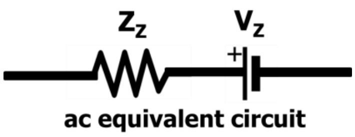


Fig 2.47

ac Equivalent circuit



Recall, diode has a dynamic resistance (r_d). Similarly, zener also has a dynamic impedance (Z_z)

Fig 2.48

Problem 2.19: A Zener has a break down voltage of 5 V and a dynamic Impedance (Z_z) =30 ohms. Zener current is 25 mA. How much will the Zener voltage change when the Zener current changes by ±10 mA? (Refer fig 2.48)

V_z = 5 V, I_z = 25 mA, ΔI_Z = ±10 mA, Z_z =30 ohms.

$\Delta V_Z = \Delta I_Z \times Z_z$ = ± 10 mA X 30 ohms = ±300 mV

V_Z (Maximum) **= V_Z + ΔV_Z** = 5 V + 300 mV = 5.3 V

V_Z (Minimum) **= V_Z - ΔV_Z** = 5 V - 300 mV = 4.7 V

2.7.5 Zener diode voltage regulator

What is a voltage regulator?

A voltage regulator ensures that the **output voltage is constant** for the following conditions.

a) **When the input voltage is varied** between a specified minimum & maximum range.

b**) When the load current is varied** from no load (0 A) to its rated full load current.

In practice, the **output voltage cannot be rock steady. It will have minor variations up and down**.

Problem 2.20: How a 5V, 200 mA regulator behaves typically, <u>when input voltage varies</u>

Voltage regulation (example)

Input voltage	12 V	10 V	8 V
Output Voltage	5.1 V	5.0 V	4.9V

Example: How a 5V, 200 mA regulator behaves typically, <u>when load current varies</u>

Current regulation

Load Current	200 mA	100 mA	0 mA (no load)
Output voltage	5.0 V	5.1 V	5.2 V

How zener diode acts as a regulator?

Refer Fig 2.49 (only reverse characteristics)

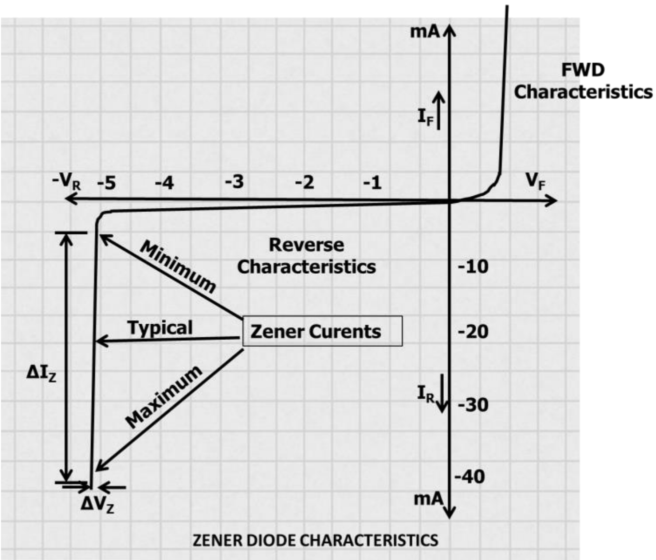


Fig 2.49

Recall, zener diode operates in the reverse bias conditions.

- **When reverse bias reaches V_Z (5 V in this example), zener break down happens and the reverse current shoots up.**
- **The zener voltage is steady around 5.0 V, even though the current varies from 2 mA to 40 mA and beyond.**
- This shows that zener can, always maintain a constant voltage across it, for a wide range of current variations through it.
- This is the property of a **good voltage regulator**

- The **zener requires a certain minimum current,** to break-down and act as a regulator. In this example, the minimum current required, is shown as 5 mA.

- Similarly, the **zener cannot support, beyond a certain maximum current**. Else, it will **exceed its maximum permissible power dissipation.** In this example, maximum current is 40 mA.
- Usually, it is prudent to **operate the zener, halfway between these two extremes.**

2.7.6 Zener diode as a shunt regulator.

Problem 2.21: Find out I, I_z and I_L for this circuit in fig 2.50

We are **sure of two nodes here**.

Node A = 12 V Node B = V_Z = 6 V

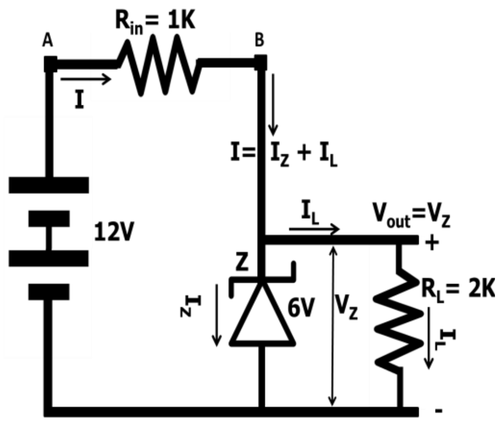


Fig 2.50

a) <u>Find I_L</u>

Voltage across R_L = Voltage of Zener

V_O = V_Z = 6 V

I_L = $\frac{V_Z}{R_L}$ = 6 V / 2K = 3 mA

b) <u>Find I (current through R_{in})</u>

One end of R_{in} is Node A and the other end is Node B. R_{in} =1 K

∴Voltage across R_{in} = V_A –V_B = 12 V – 6 V = 6 V.

Current through R_{in} = 6 V / 1K = 6 mA

c) <u>Current thro Zener</u>

I = I_Z + I_L

6 mA = I_z + 3 m A

∴ I_Z = 3 m A.

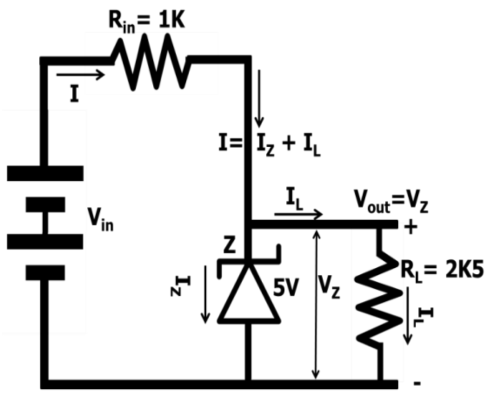


Fig 2. 51

Problem 2.22: Calculate the input voltage range for which output will be constant, for the circuit in fig 2.51. The zener must operate between 5mA and 20mA.

R_L = 2.5 K, V_z = 5

∴ I_L = 5 V / 2.5 K = 2 mA. Note I_L is always 2 mA in this circuit.

<u>1) Calculate V_{in} min</u>	<u>2) Calculate V_{in} max</u>
V_{in} min happens when I_Z is min = 5 mA	**V_{in} max happens when I_Z is max** = 20 mA.
I = I_L + I_Z min = 2 mA + 5 mA = 7 mA	I = I_L + I_Z max = 2 mA+20 mA = 22 mA
∴The current thro R_{in} = I = 7 mA	∴The current thro R_{in} = I = 22 mA
Voltage drop across R_{in} = I X R_{in} = 7 mA X 1K	Voltage drop across R_{in} = I X R_{in} = 22 mA X1 K

$= 7\ V$ $\therefore V_{in}$ (min) required $=$ Voltage across $R_{in} + V_Z$ $= 7\ V + 5\ V = 12\ V$	$= 22\ V$ …V_{in} (max) $=$ Voltage across $R_{in} + V_Z$ $= 22\ V + 5\ V = 27\ V$.

Problem 2.23: The zener in fig 2.51(a), is required to deliver a load current of 20 mA at a constant output voltage of 6 V. The minimum current of the zener is 5 mA. P_D max of zener is 240 mW. The input varies between 10 V to 12 V. What should be the value of the series limiting resistor?

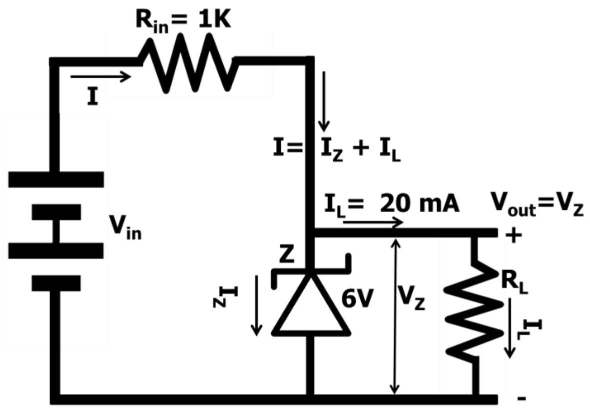


Fig 2.51(a)

$V_{out} = 6\ V = V_z$, P_D max = 240 mW,
I_Z min = 5 mA, Input : 10 V to 12 V, I_L =20 mA

1) <u>To find I_z max</u>

I_z min = 5 mA (given) but what is Iz max?
P_D max = 240 mW (given).
P_D = I_z max X V_Z
240 mW = I_z max X 6 V
I_z max = 40 mA

2) <u>To find I_{max} and I_{min}</u>

I_{max} = I_z max + I_L = 40 +20 = 60 mA
I_{max} = I_z min + I_L = 5 + 20 = 25 mA

3) <u>To find R_{min}</u>

R_{min} happens when when V_{in} is max and I is Imax

V_{in} (max) = $V_z + I_{max} R_{min}$
12 V = 6 V + 60 mA X Rmin

$\therefore$ **R_{min}** $= \frac{6\ V}{60\ mA}$ = **100 Ω**

4) To find R_{max} ?

R_{max} happens when V_{in} is minimum and I is I_{min}

V_{in}(min) = V_z + Imin R_{max}
10 V = 6 V + 25 mA X R_{max}

R_{max} $= \frac{4\ V}{25\ mA}$ = **160 Ω**

$\therefore$The value of R should be between 100 Ω and 160 Ω.

<u>Relationships to remember.</u>

1. **How to find I_z max?** Use the relation: $P_D = I_z$ max X V_Z
2. **How to find I_{max} and I_{min}?** Use the relation $I_{max} = I_z$ max+I_L & $I_{max} = I_z$ min+ I_L.
3. **How to find R_{min}?** R_{min} happens when when V_{in} is max and I is Imax
4. **How to find R_{min}?** R $_{max}$ happens when V_{in} is min and I is I_{min}
5. **How to find V_{in} max and V_{in} min?** Use the relations V_{in} (max) $= V_z + I_{max} R_{min}$ and V_{in}(min) $= V_z + I_{min} R_{max}$

2.8 Series and shunt diode clipping circuits

What is clipper?

- A circuit, which **removes unwanted segments of a wave-form, is called a clipper.**
- A clipper is also known as **a limiter**.
- A **half wave rectifier is an example** of clipper which clips one half cycle of the input.
- Diodes are used in clippers.
- If the diode is **in series with the load, it is called a series clipper**.
- If the diode is **in parallel with the load, it is called a parallel clipper.**

2.8.1 Series clippers (refer fig 2.52)

The diode is series with the load.

If the **+ ve part of the input signal is clipped off, it is a +ve clipper**.

If the **– ve part of the input signal is clipped off , it is a –ve clipper.**

Series –ve clipper (Silicon Diode)

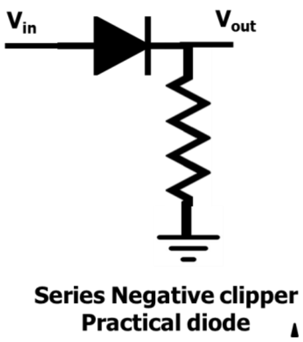


Fig 2.52

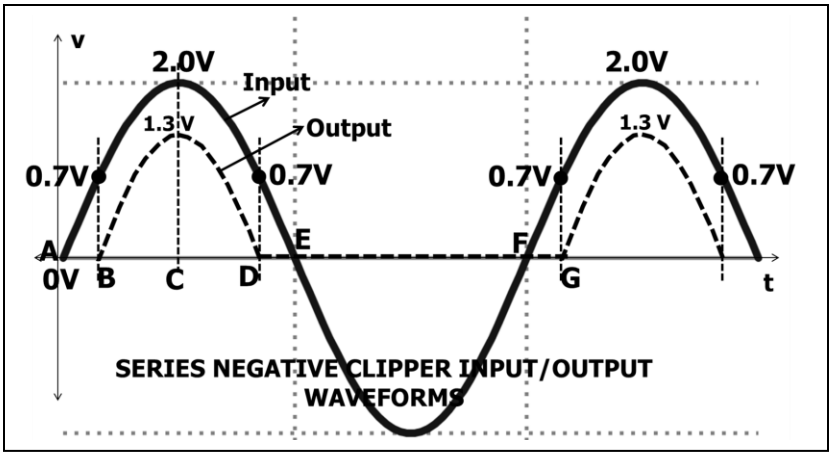


Fig 2.53

Look at the cicuit diagram (fig 2.52) and the wave form (fig 2.53). Assume Silicon diode.

Input : Solid sine wave. **Output :** Dotted sine wave .

A ➔ Input is at 0 V.

Diode has zero bias. (Anode is at 0 V and cathode also is at 0 V through the qrounded R_L).

$\therefore$ Diode does not conduct (cut off)

B ➔ Input is at 0.7 V.

Diode is FWD biased (Anode is at 0.7 V and cathode is at 0 V).

Output is $V_{in} - V_F$ = 0.7 V - 0.7 V = 0 V.

Diode begins to conduct.

C ➔ Input is at its peak 2 V.

Diode continues to be forward biased.

Output is $V_{in} - V_F$ = 2 V - 0.7 V = 1.3 V.

D ➔ Input has reduced back to 0.7 V.

Diode is still fwd biased.

Output is $V_{in} - V_F$ = 0.7 V - 0.7 V = 0

Diode is about to cut-off..

E ➔ Input = 0 V. Diode is zero biased, as at A. Diode is cut off. Output is at 0 V (since R_L is grounded).
E to F ➔ The input is less than 0V.Diode is reverse biased and cut off . Output is 0 V.
.
It is clear from the above that the diode, conducts during **major portion of +ve input cycle** and is cut off **entirely during –ve input cycle. The output follows input, during +ve input cycle and is clipped during –ve input cycle. ∴it is a –ve clipper.**

Note that there is **a 0.7 V difference, between input & output**, due to silicon diode drop of 0.7 V.
If we assume an **ideal diode**,

the **input & output wave forms will be exactly the same** (VF =0), during +ve cycle (A to E) and

the output will be zero, during –ve cycle from E to F.

Similar wave forms are shown for triangular and square waves, **assuming ideal diode**. (refer fig 2.54)

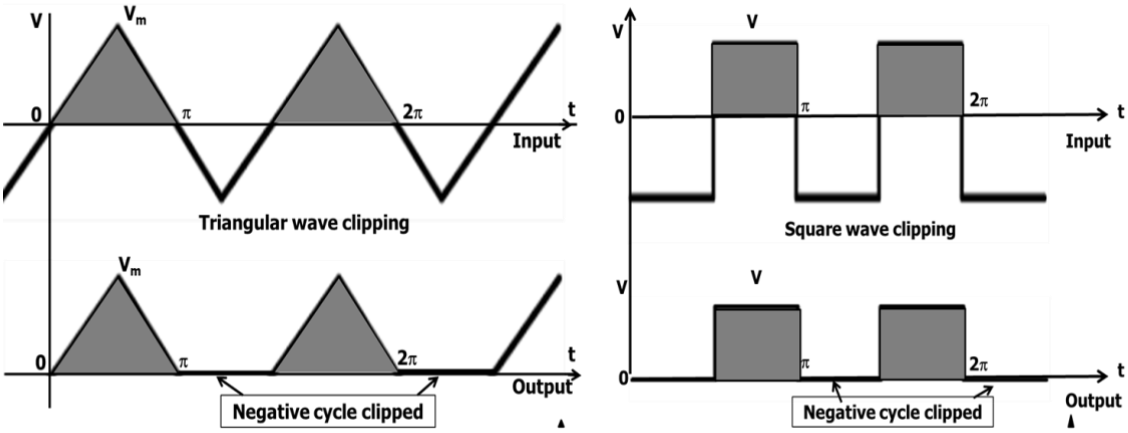


Fig 2.54 Clipper waveforms for triangular and square wave inputs

2.8.2 Transfer characteristic (–ve clipper)
What is a transfer characteristic?
Refer fig 2.55. It is the relationship between the output and input, of an electronic circuit like a clipper, for example.

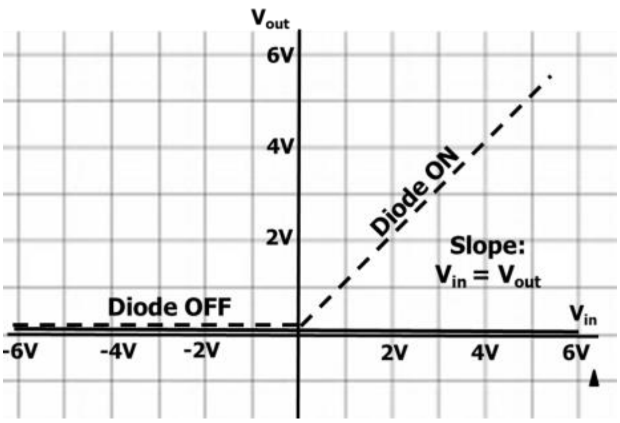


Fig 2.55 Transfer characteristics

The solid line is the input. The dotted line is the output. (the lines actually should coincide but are shown close to each other, for easy under standing

During the +ve input cycle
As input varies between, 0 and + 6 V, output also varies from 0 V to + 6 V. (o/p follows i/p).

During the -ve input cycle

As input varies between 0 and – 6 V, output also remains at 0 V (clipped)

$V_o = V_{in}$ (for $V_{in} \geq 0$ V.)

$V_o = 0$ (for $V_{in} < 0$ V.)

Series positive clipper (Ideal diode)

Circuit diagram:

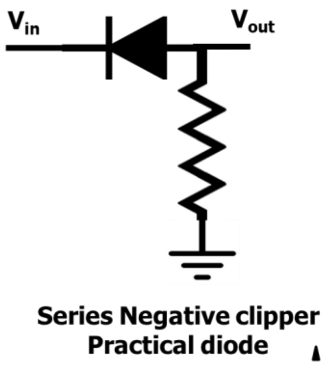


Fig 2.56

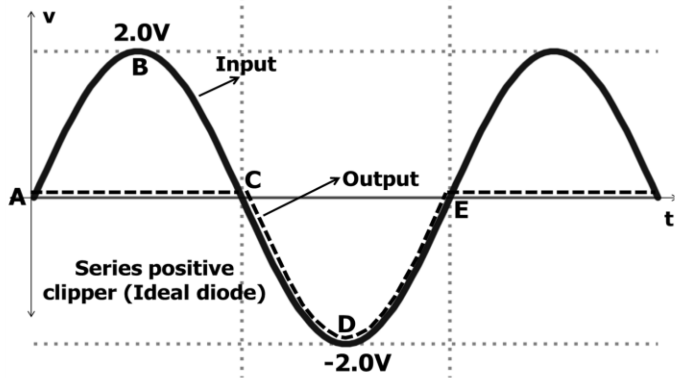


Fig 2.57

+ve clipper is similar to -ve clipper, except that the diode is reversed.

Refer circuit diagram (fig 2.56) and waveforms (fig 2.57) shown.

The dotted line is the input. The solid line is the output. (the lines actually should coincide but are shown close to each other, for easy under standing

A → Input (V_{in}) = 0 V. Diode is zero biased. Anode is at 0 V and cathode is at 0 V. **Diode is cut off**. Output is at 0 V.

B → Input (V_{in}) = 2 V. Diode is reverse biased . Anode is at 0 V and cathode is at 2 V. **Diode is cut off .** Output is at 0 V.

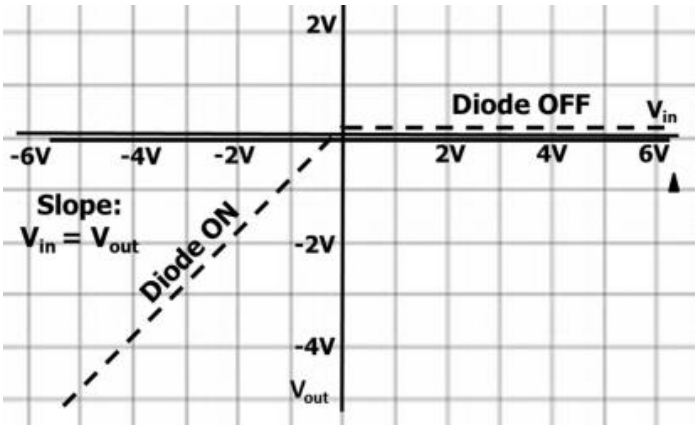
C → Same as A. Output is at 0 V.

D → V_{in} = - 2 V. The diode is forward biased. **Cathode is more –ve with respect to anode**. **Diode conducts. Output follows input**

E → Same as A and C. Output is at 0 V.

It is clear from the above, that the output is zero during +ve input cycle (A to B to C) and output follows input during –ve input cycle (C to D to E). Positive cycle is clipped & hence it is a +ve clipper..

Transfer characteristic (+ve clipper)



Fiig 2.58

$V_o = 0$ for $V_{in} > 0$ V

$V_o = V_{in}$ for $V_{in} \leq 0$ V

Problem 2.24: For the series clipper in fig 2.59 sketch input & output wave forms. If the resistor value is 1k5 (1.5k), what is the load current? Assume Silicon diode (V_F = 0.7 V)

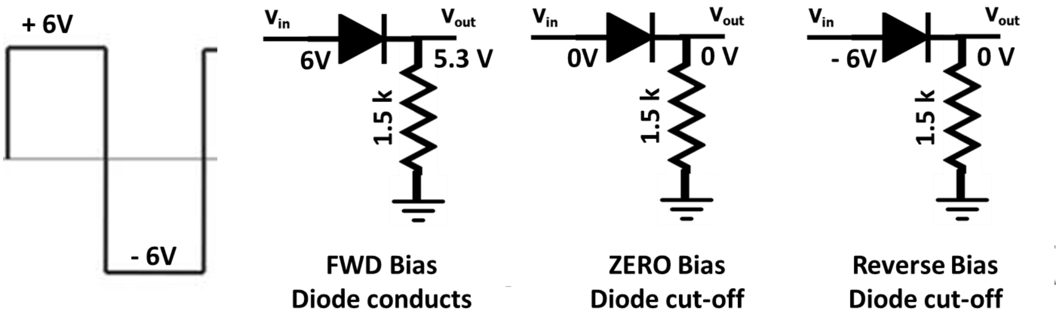


Fig 2.59

The three conditions are shown in fig 2.59 and the input and output wave forms are as shown in fig 2.60.

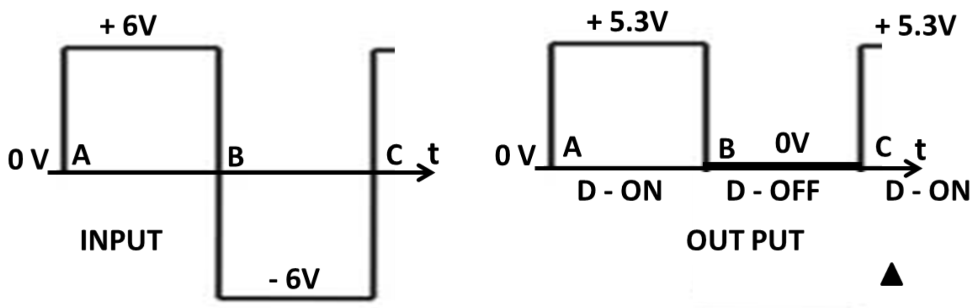


Fig 2.60

Load current $I_L = \frac{\mathbf{V_{out}}}{\mathbf{R_L}} = \frac{\mathbf{5.3\ V}}{\mathbf{1.5\ k}}$ = 3.53 mA.

2.8.3 Series Noise clipper

Refer figure 2.61.and 2.62. This is a series noise clipper. Two diodes, are connected back to back, in a parallel fashion. Let us assume both are silicon diodes.

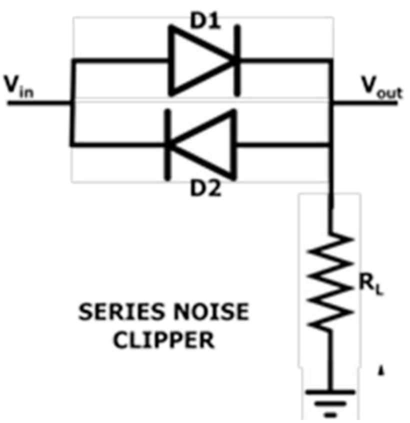


Fig 2.61

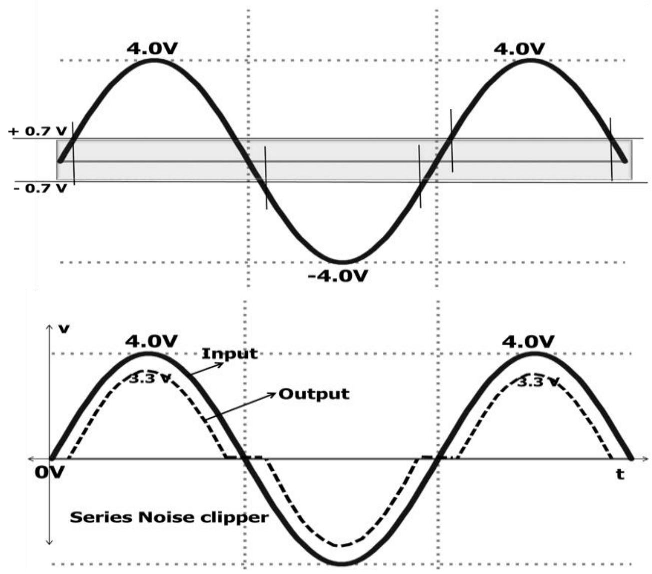


Fig 2.62

1) V_{in} is between + 0.7 V and – 0.7 V

Diodes D1 is not forward biased. D2 also is not forward biased.
D1 & D2 remain cut off. $V_{out} = 0$

2) Vin = ≥ +0.7 V.

Diode D1 is fwd biased and diode D2 is rev biased. D1 conducts. D2 is cut off. $V_{out} = V_{in}$ (+ve cycle)

3) Vin = ≤ – 0.7 V.

Diode D1 is rev biased and diode D2 is fwd biased. D2 conducts. D1 is cut off. $V_{out} = V_{in}$ (-ve cycle).

Where is this clipper used?

In communication technology, very often, signals have a constant low level noise built in. For good reception, this low level noise, needs to be cleaned up. Series noise clipper is used in such situations. (Refer fig 2.63)

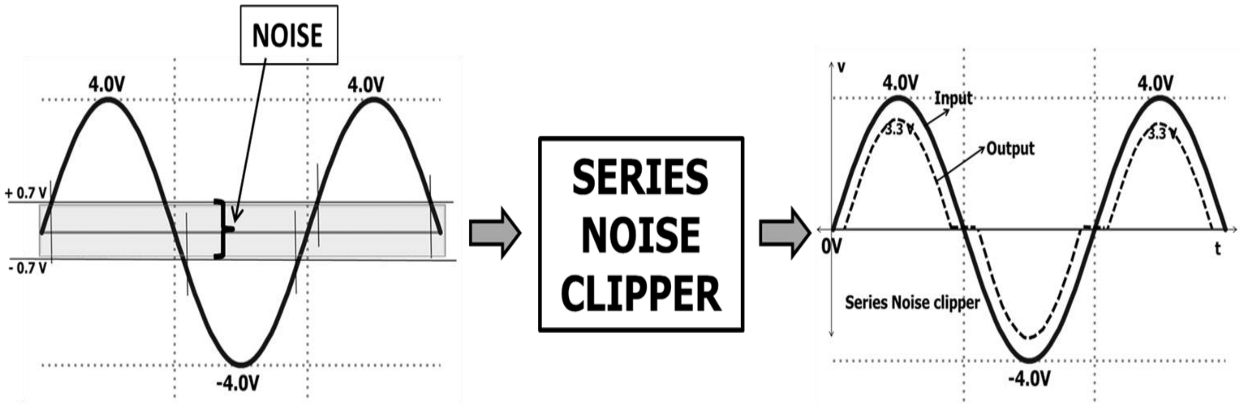


Fig 2.63

The output has no noise, as long as the input noise is within ± 0.7 V. Of course, the output amplitude will be less by ± 0.7 V and there will be "no-conduction" zones.

2.8.4 Shunt clippers (Parallel Clippers)

Circuit diagram is shown in fig 2.64

Positive shunt clippers

Refer fig 2.64. Assume an ideal diode ($V_F = 0$, $R_F = 0$)

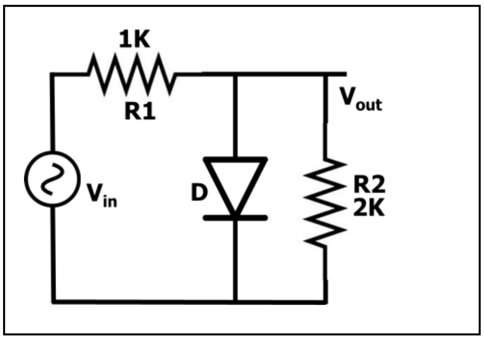


Fig 2.64

Negative input cycle (fig 2.65)

When $V_{in} < 0$ V, the diode is reverse biased. The diode is cut off and becomes an open circuit.
It is, as if, the diode is not there at all.
Therefore V_{out} follows V_{in} for the entire –ve cycle.

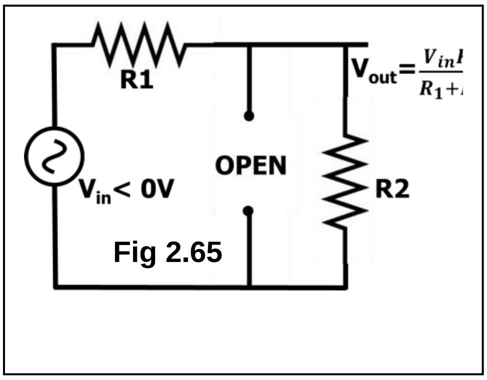


Fig 2.65

+ve input cycle (fig 2.66)

When $V_{in} \geq 0$V, the diode is forward biased. Diode conducts and forms a short ckt. [Ideal diode $V_F = 0$ V)

The output is 0 V during the entire +ve cycle. Therefore +ve cycle Is clipped.

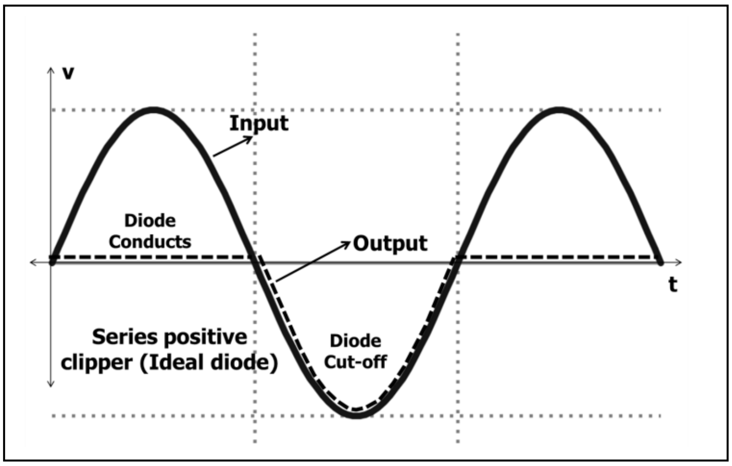


Fig 2.67

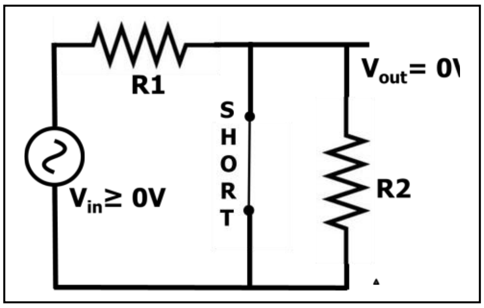


Fig 2.66

Please note that unlike a series clipper, V_{out} will not be equal to V_{in}. There are two resistors R1 and R2 involved in this circuit.

Therefore $V_{out} = \frac{V_{in}R_2}{R_1+R_2}$ (R1 and R2 are potential dividers)

Problem 2.25: What is the output wave form of the clipper in fig 2.68? Assume silicon diode (V_F = 0.7 V)

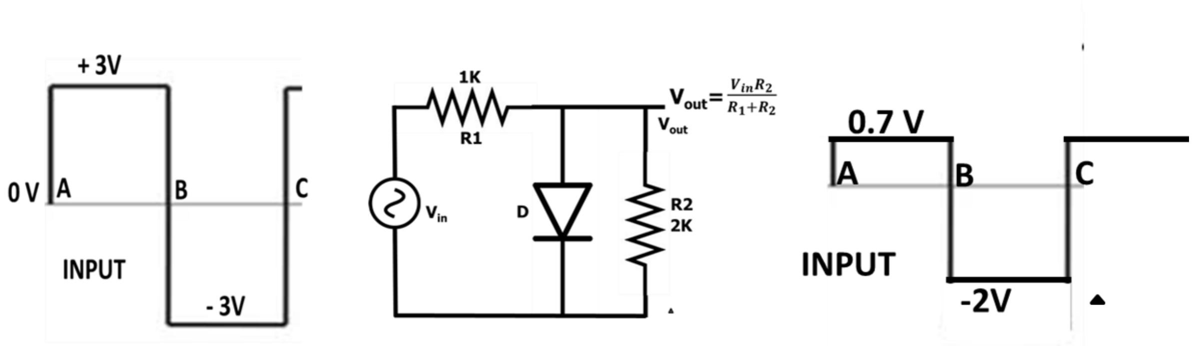


Fig 2.68

Input = +3 V.
Diode conducts .
Therefore output is restricted to
V_F =0.7 V_{out} =0.7V.

Input = ─ 3 V.
Diode is cut off

$\therefore V_{out} = \frac{-V_{in}R_2}{R_1+R_2} = \frac{-3X2k}{1k+2k}$ = -2 V.

O/P wave form is shown in fig 2.68.

Transfer characteristics.

Refer fig 2.69.

$V_{in} \geq 0$ V $\quad V_o = 0$

$V_{in} < 0$ V $\quad V_{out} = \frac{V_{in}R_2}{R_1+R_2}$

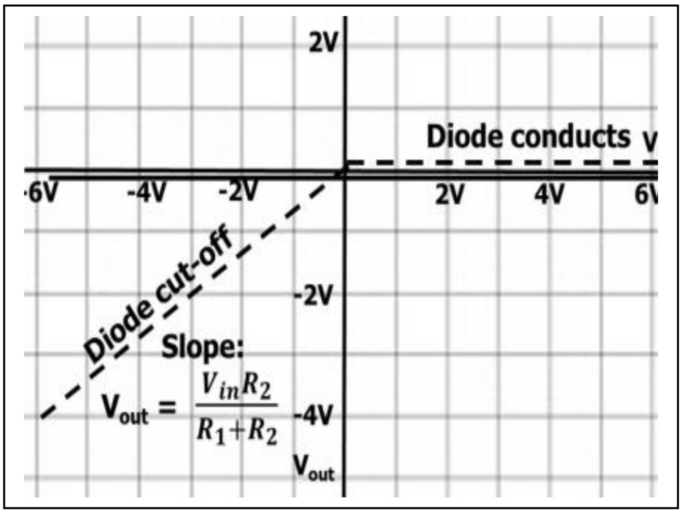


Fig 2.69 Transfer characteristics

2.8.5 Negative shunt clippers

Refer circuit diagram 2.70. It is similar to parallel +ve clipper, except that the diode is reversed. Again assume an ideal diode (V_F = 0 V, R_F = 0 Ω)

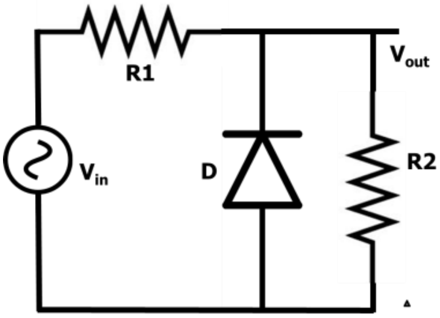


Fig 2.70 Negative clipper

Negative clippers

- ve input cycle

- When V_{in} < 0 V, the diode is forward biased.
- Diode conducts and forms a short ckt. [Ideal diode V_F = 0 V]
- The output is 0 V during the entire -ve cycle.
- Therefore -ve cycle Is clipped.

+ve input cycle

- When V_{in} ≥ 0V, the diode is reverse biased.
- The diode is cut off and becomes an open circuit.
- It is as if, the diode is not there at all.
- Therefore V_{out} follows V_{in} for the entire –ve cycle.

Please note that unlike a series clipper, V_{out} will not be equal to V_{in}. There are two resistors R1 and R2 involved in this circuit. The waveforms are shown in fig 2.72

Therefore $V_{out} = \frac{V_{in}R_2}{R_1+R_2}$ (R1 and R2 are potential dividers)

Transfer characteristics (fig 2.71)

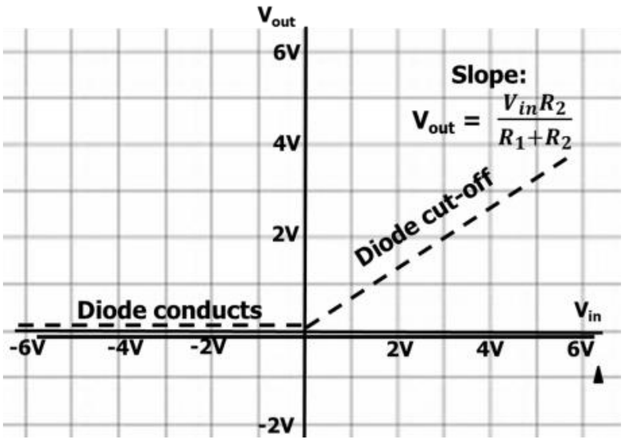


Fig 2.71 Transfer Characteristics

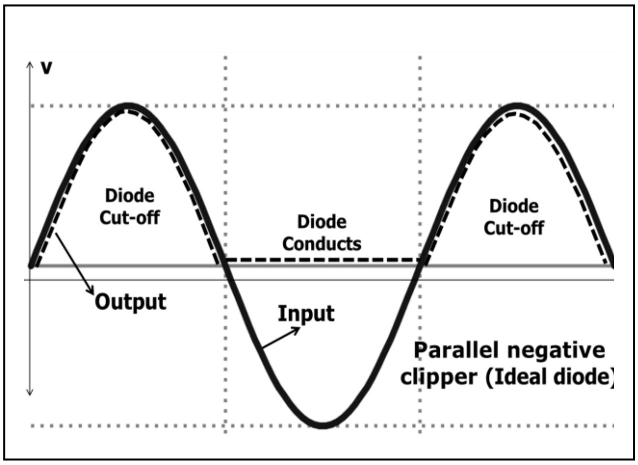


Fig 2.72

V_{in} ≥ 0 V $\quad V_{out} = \frac{V_{in}R_2}{R_1+R_2}$

V_{in} < 0 V $\quad V_o = 0$

2.8.6 Shunt Noise clipper (Using Germanium Diodes)

Refer fig 2,73 for circuit diagram. Assume germanium diodes. (V_F = 0.3 V)
Look at input wave form. It has ripples (noise) between + 1.5 V & + 2.0 V and also between -1.5 V and -2.0 V..

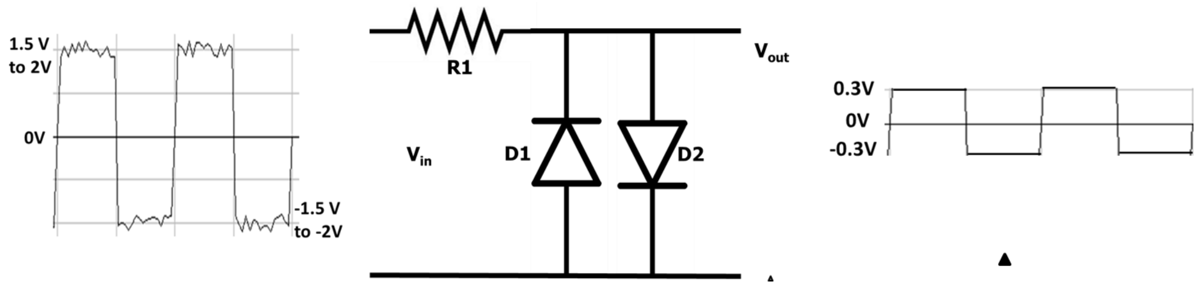


Fig 2.73 Shunt Noise Clipper

There are two diodes (Ge) connected back to back.
If the input is V_{in} ≥ 0.3 V, diode D2 conducts and clips the output to + 0.3 V.
If the input is V_{in} ≤ - 0.3 V, diode D1 conducts and clips the output to -0.3 V.
The output is a clean square wave of ± 0.3 V, without any noise ripples. Hence this circuit is called a noise clipper. The waveforms are shown in fig 2.73.

2.8.7 Biased Clippers

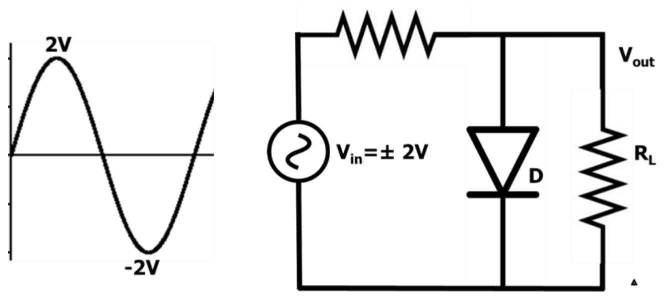


Fig 2.74 Biased Clipper

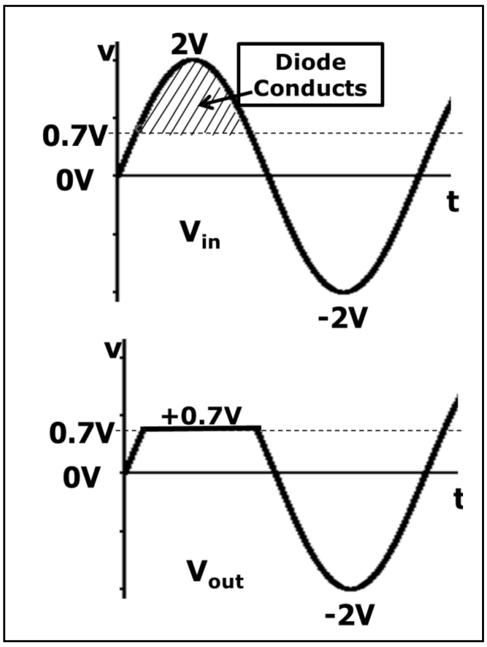


Fig 2.75 Clipper waveform

Example 1: What is the output of this clipper in fig 2.74? (silicon diode, V_F = 0.7V)

1) The diode will start conducting when the input is ≥ + 0.7 V. The output will be clipped at + 0.7 V, once the diode starts conducting.

2) Diode will stop conduction, when the input n < + 0.7 V. The output will be following input, once the diode stops conducting. Therefore, it is a +ve clipper. The waveforms are shown in fig 2.75.

Example 2: What is the output of this clipper in 2.76? (silicon diode, V_F = 0.7V)?

1) The diode will start conducting when the input is ≤ - 0.7 V. (Anode is at 0 V and cathode is negative by 0.7 V.) The output will be clipped at - 0.7 V, once the diode starts conducting.

2) Diode will stop conduction, when the input is > - 0.7 V. The output will be following input, once the diode stops conducting.

Therefore, it is a - ve clipper. The output waveform is shown in fig 2.76

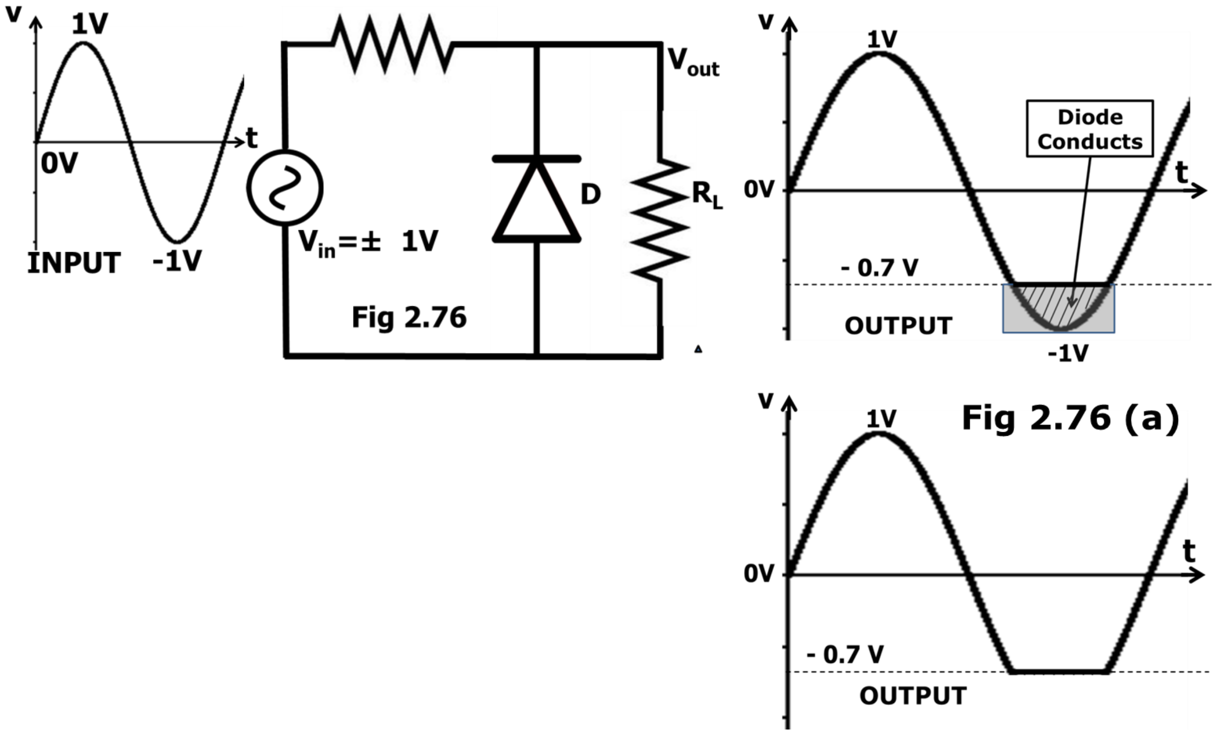


Fig 2.76

Fig 2.76 (a)

Problem 2.26: What is the output of this clipper in fig 2.77? (silicon diode, V_F = 0.7V)

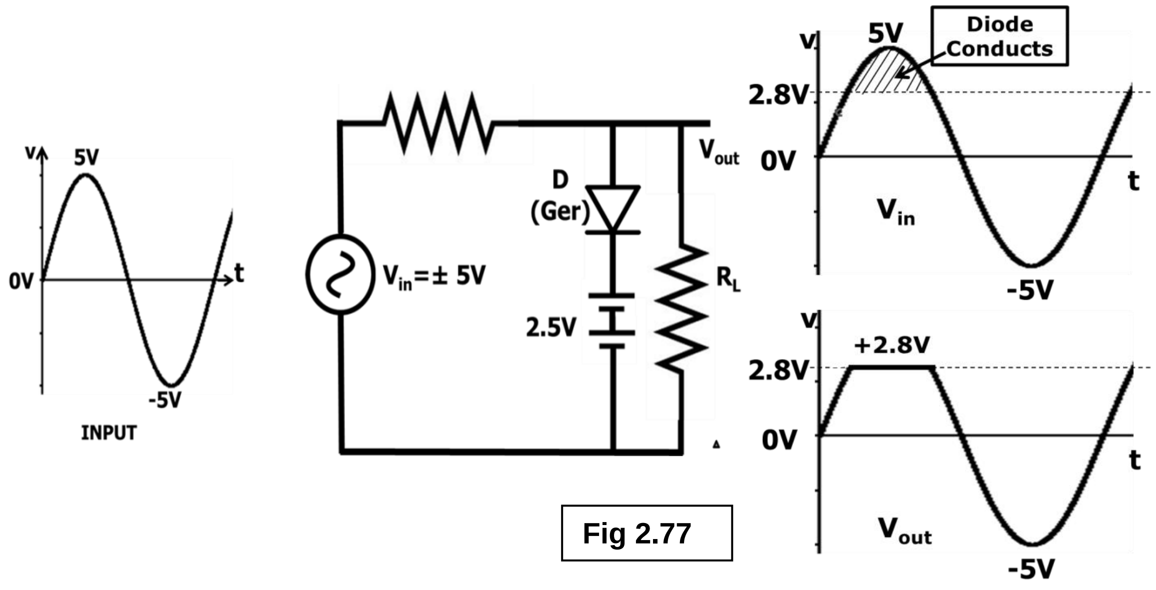


Fig 2.77

Diode cathode is biased at +2.5 V.
Diode will conduct, if and only if its anode is 0.3 V (germanium) more.
In other words, when input is ≥ 2.8 V, diode conducts and keeps the output clipped at 2.8 V.
When input is < 2.8 V, diode is open and the output follows input
Waveform is shown in fig 2.77

Problem 2.27: What is the output of this clipper in 2.78? (silicon diode, V_F = 0.7V)

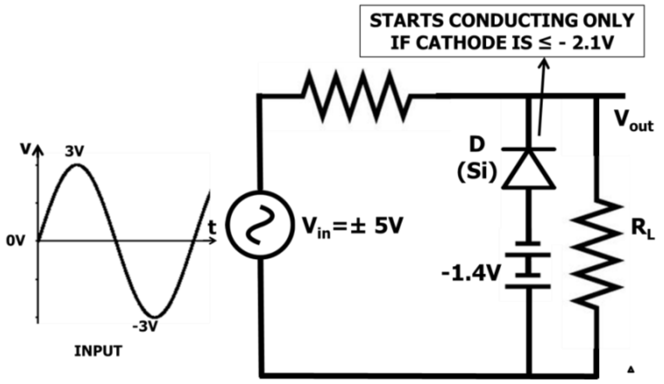


Fig 2.78

. Diode`anode is at - 1.4 V.

Diode will conduct if and only if its cathode is more negative by 0.7 V than its anode. i.e. ─ 1.4 V ─ 0.7 V = ─ 2.1 V.

Wave form is shown in fig 2.79.

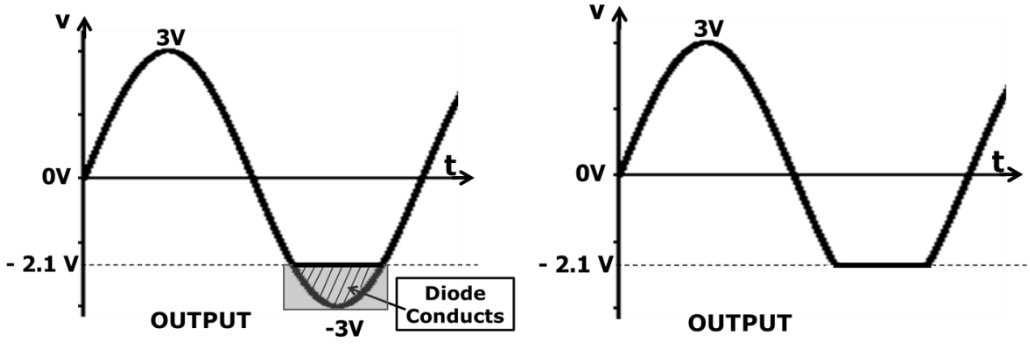


Fig 2.79

Double clipping (Refer fig 2.80)

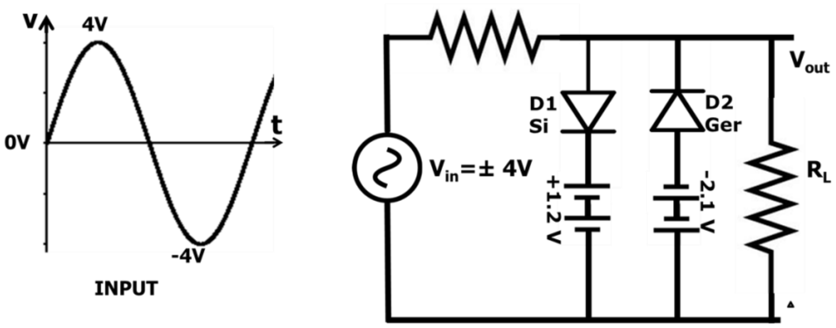


Fig 2.80 Double clipper circuit

D1 conducts if
V_{in} ≥ + 1.2 V + 0.7 V =1.9 V. (Silicon)

D2 conducts if
V_{in} ≤ - 2.1 V - 0.3 V = -- 2.4 V (Germanium).
Wave form in fig 2.81

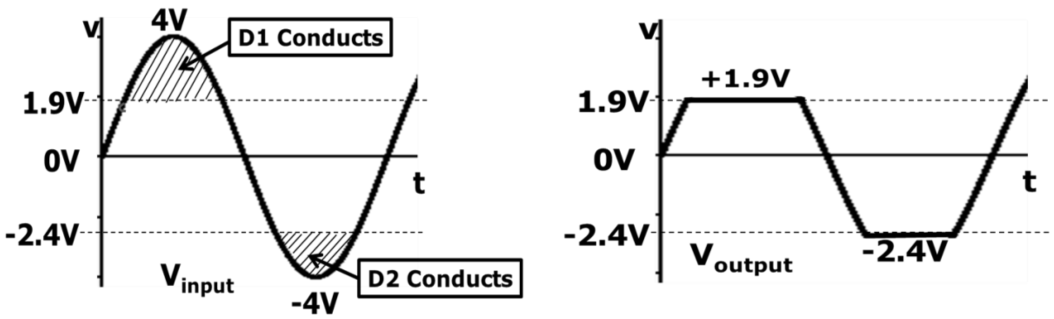


Fig 2.81 Double clipper waveform

2.9 Clamper circuits

In telecommunication, very often wireless propagation is involved, using antennae. .In wireless communication, DC information cannot be propagated and is lost. At the receiver, in order to get back the original signal, the DC that was lost, needs to be restored. Therefore we need circuits, which can shift DC up or down .These circuits are known as clampers. One huge application is, in TV receivers where DC is restored, to maintain the video signal at appropriate black levels & white levels.
A negative clamper is shown in fig 2.82.

2.9.1 Negative clamper:

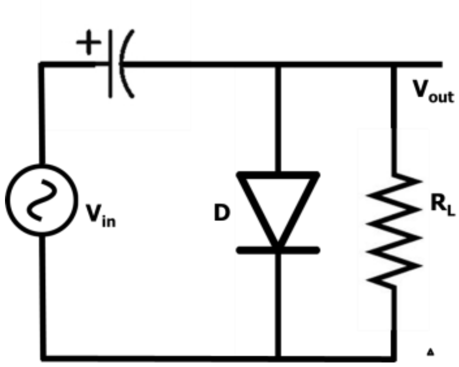


Fig 2.82 Negative clamper circuit

The clamper has a series capacitor. We have already seen a similar negative clipper circuit, using a series resistor instead of a series capacitor.

The clamper circuit always uses a capacitor. Let us illustrate how clamper works, through a series of diagrams. Let us assume ideal diode (V_F= 0 R_F= 0).

What happens during the first +ve half cycle (0 to 90 deg)? Refer 2.82

During the first quarter cycle (0 to 90 deg), the input rises from 0 to 5 V and the capacitor charges to +5 V.
The diode, conducts in this duration, since it gets forward biased. (Anode is at >0 V and cathode is at 0 V.)
Diode acts like a short and output remains zero in this duration.

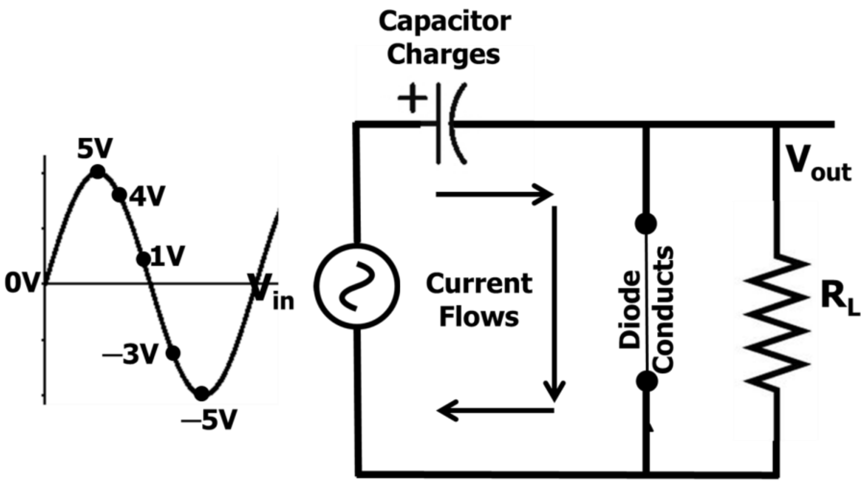


Fig 2.83. Capacitor acts like a battery

The capacitor will hold this 5 V since, it does not usually have a quick discharge path.

We can therefore replace the capacitor, by a battery (please note down the polarity of the voltage, across the capacitor).

2.9.2 Clamping action

How clamping action take place?

Look at the figure 2.83 (a). Let **us replace the capacitor by a 5 V battery** (look at the polarity).

Let us analyse the clamping action through a series of few simple static equivalent circuits shown in figures 2.83 (b) to 2.83 (f).

The instantaneous voltages shown in $V_{in,}$ in fig 2.83 (a) are replaced by batteries in these circuits (for easy under-standing).

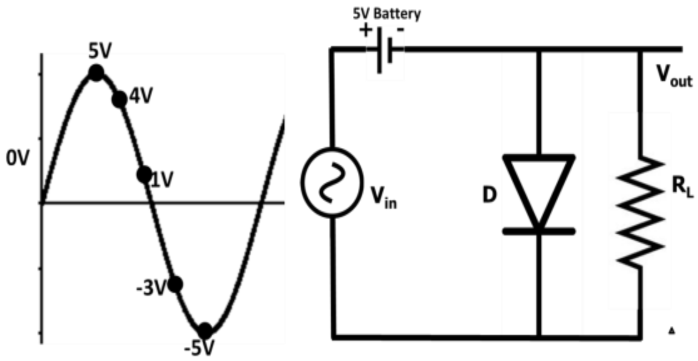


Fig 2.83 (a)

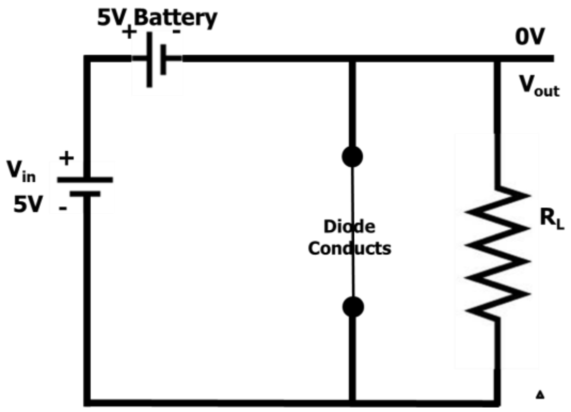
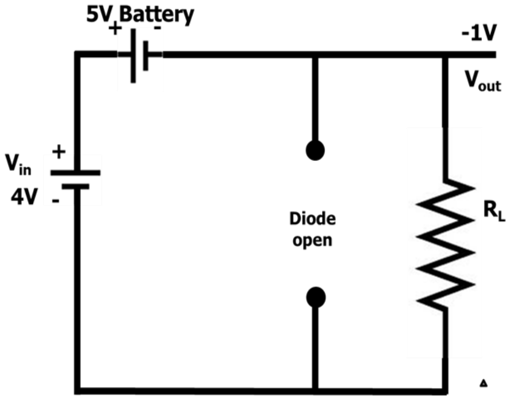
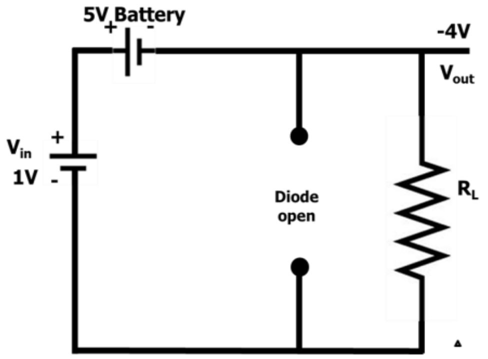


Fig 2.83 (b)



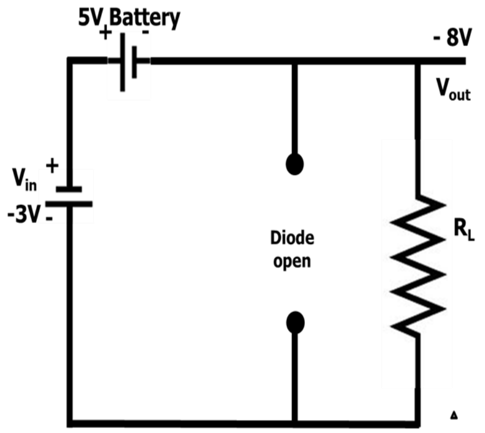
V_{in} = 4V.
Batteries oppose each other.
Diode is reverse biased and becomes open
V_{out}= +4V – 5V = -1V

Fig 2.83 (c)



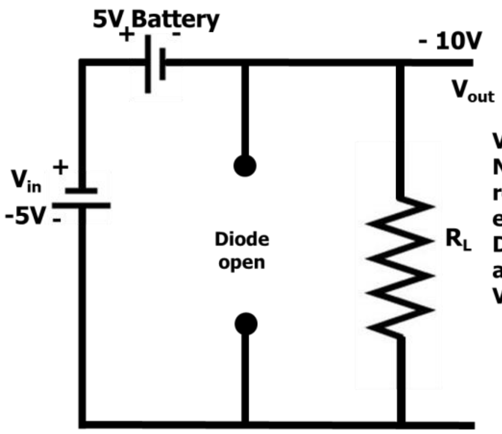
V_{in} = 1V.
Batteries oppose each other.
Diode is reverse biased and becomes open
V_{out}= +1V – 5V = -4V

Fig 2.83 (d)



V_{in} = -3V.
Note battery polarity is reversed
Batteries assist each other.
Diode is reverse biased and is open
V_{out}= -3V – 5V = -8V

Fig 2.83 (e)



V_{in} = -5V.
Note battery polarity is reversed. Batteries assist each other.
Diode is reverse biased and is open
V_{out}= -5V – 5V = -10V

V_{in} (V)	V_{out} (V)
5	0
4	-1
1	-4
-3	-8
-5	-10

Fig 2.83 (f)

The waveforms are shown in fig 2.84 and the results are tabulated here.

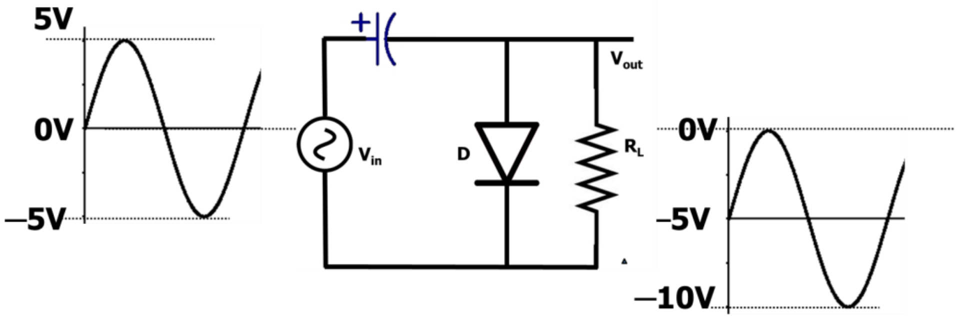


Fig 2.84 Negative clamper Input/Output characteristics

The input range of +5 V to – 5 V, has been shifted down to 0 V to -10 V. Hence it is a negative clamper.

2.9.2 Positive clamper (Ideal diode)

Operation

Refer fig 2.85(a). Note the polarity reversal of the capacitor.

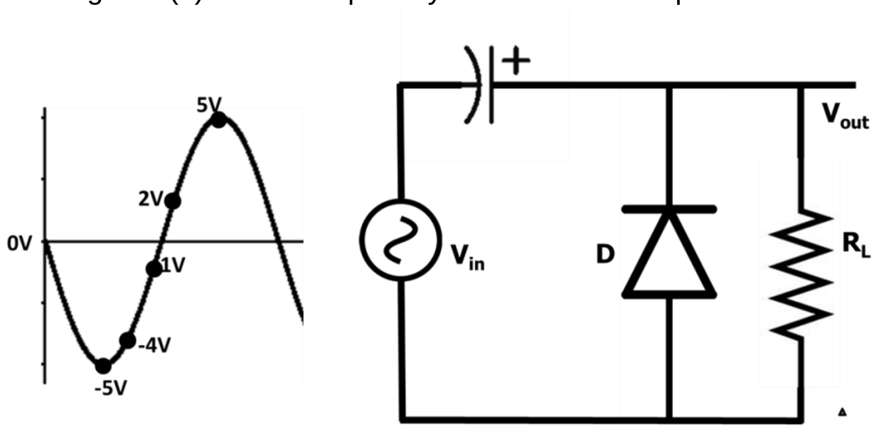
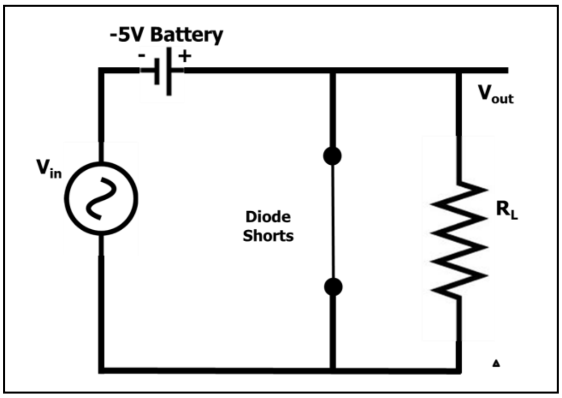


Fig 2.85 (a)

During the first quarter cycle (0 to 90 deg), the input varies from 0 to -5 V and the capacitor charges to -5V.

The diode conducts in this duration, since it gets forward biased. (Anode is at 0V and cathode is more negative with respect to anode.)



Diode acts like a short and output remains zero in this duration (fig 2.85 (b))

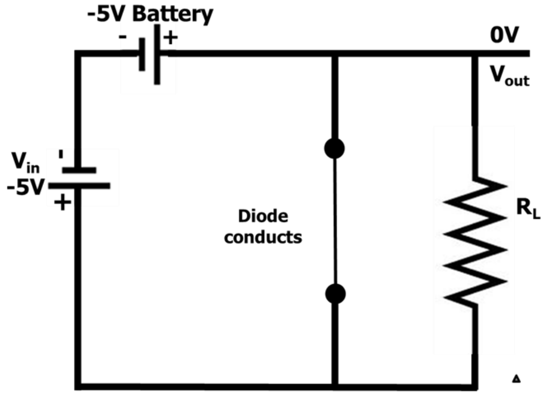
.

The capacitor will hold this -5 V since, it does not usually have a quick discharge path. We can therefore replace the capacitor, by a battery (please note the polarity of the voltage, across the capacitor).

Let us analyse the clamping action through a series of few simple static equivalent circuits, shown in figures 2.85 (c) to 2.85 (f)..

The instantaneous voltages shown in $V_{in,}$ are replaced by batteries in these circuits (for easy under-standing).

Refer figures 2.85 (c) to (f). The analysis is similar to that of negative clamper except that the polarities of signals and battery voltages are changed.



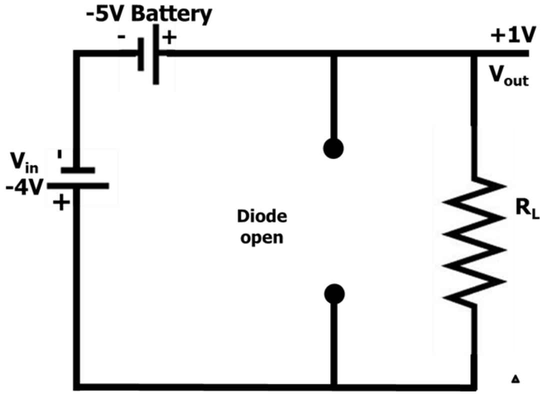
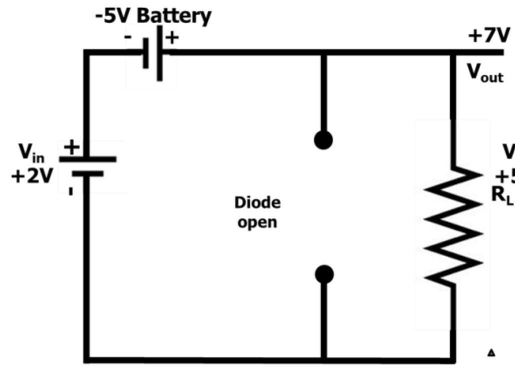


Fig 2.85 (c) **Fig 2.85 (d)**



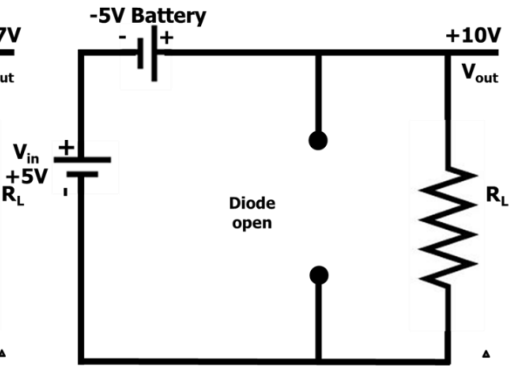


Fig 2.85 (e) **Fig 2.85 (f)**

The clamper waveform is shown below in fig 2.86. The results are tabulated here.

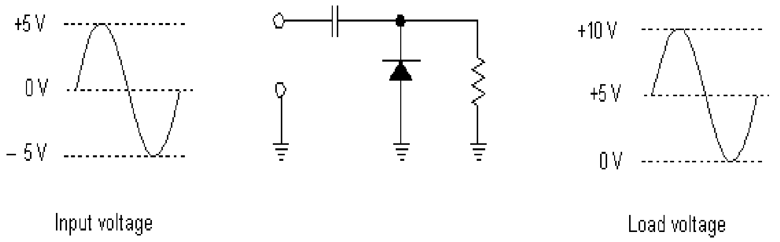


Fig 2.86 Negative clamper Input Output characteristics

V_{in} (V)	V_{out} (V)
-5	0
-4	+1
0	+5
+2	+7
+5	+10

Problem 2.28: Design a - ve clamper with a silicon diode (V_F = 0.7 V). What will be the output, for an input signal of ± 3 V.
In the previous section the diode was assumed to be an ideal diode. Now we have a practical diode, with V_F = 0.7 V.

Refer fig 2.87. During the first quarter of the input cycle, the voltage rises from 0 V to +3 V.
V_{out} starts following the input (capacitor couples input signal to output)
The diode gets forward biased when the input is ≥ 0.7 V. (Refer negative clamper theory)
.

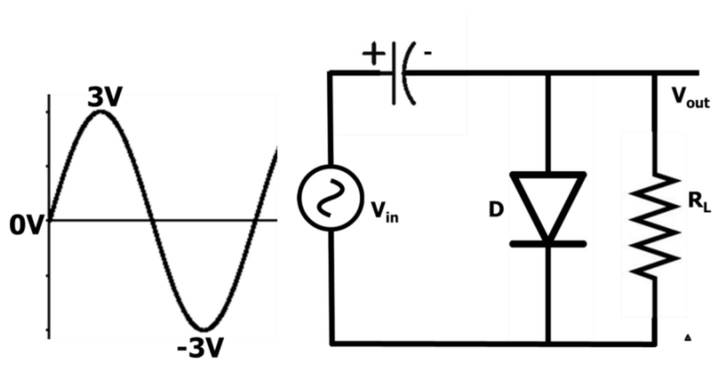


Fig 2.87

Once the diode conducts, V_{out} becomes 0.7 V (In the previous section, V_{out} was 0 V, since the diode was ideal).

Vin = ±3 V (given)

When input reaches +3 V, the +ve plate of the capacitor is +3 V and the negative plate of the capacitor is 0.7 V. Therefore, the voltage across capacitor is 3 V – 0.7 V = 2.3 V.

Voltage across capacitor = 3 V – 0.7 V = 2.3 V.

Now onwards, follow the same explanation as in the previous section, except that the capacitor should be replaced by, an equivalent battery of 2.3 V (instead of 5.0 V battery as in previous section), as shown in figure 2.88.

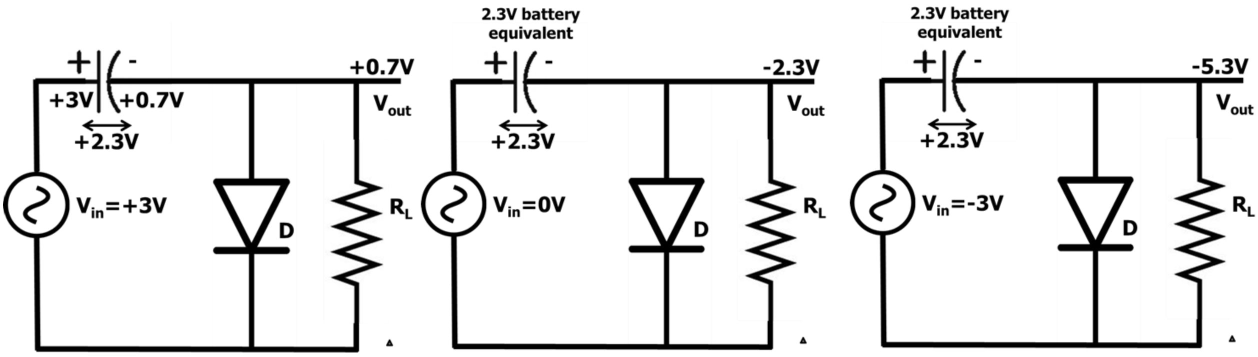


Fig 2.88 Negative clamper Input Output characteristics

The output swings between + 0.7 V and – 5.3 V as seen below. The waveforms are shown in fig 2.89

1) V_{in} = +3 V
   V_{out} = +3 V - 2.3 V = +0.7 V
2) V_{in} = 0 V
   V_{out} = 0 V - 2.3V = -2.3 V
3) V_{in} = --3 V
   V_{out} = -3 V - 2.3 V = --5.3 V

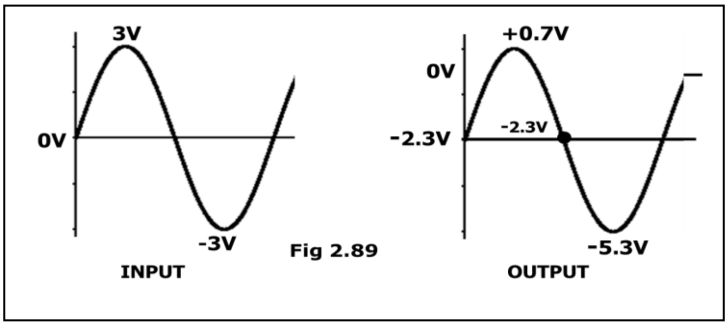


Fig 2.89

The circuit has clamped the input by -2.3 V. It is a negative clamper.

2.9.3 Diode's role

The diode conducts only during the first quarter cycle of the input. Refer fig 2.90. After that the diode never conducts (assuming an ideal diode and ideal capacitor which never loses char**ge)**

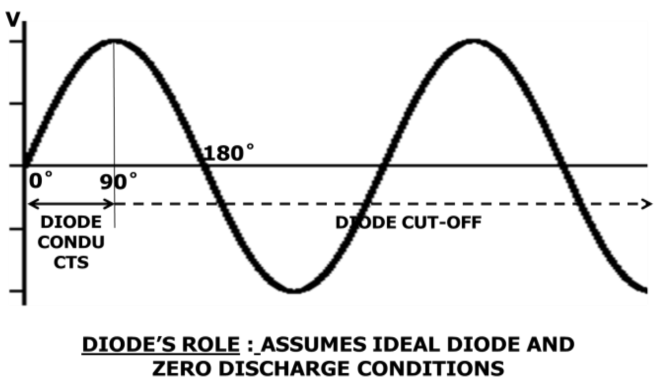


Fig 2.90

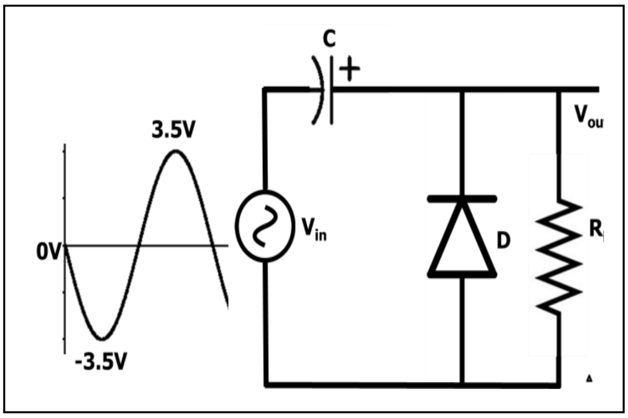


Fig 2.91

Problem 2.29: Design a +ve clamper, with a germanium diode (V_F = 0.3 V). What will be the output, for an input signal of ± 3.5 V?

Refer fig 2.91. During the first quarter of the input cycle, voltage swings from 0 V to -3.5 V.

Therefore, V_{out} starts following the input (capacitor couples input signal to output)
When the input is less than - 0.3 V, the diode gets forward biased (refer positive clamper theory).
Once the diode conducts, V_{out} gets clamped to -0.3 V (In the previous section, V_{out} was + 0.7 V, since the diode was silicon and the circuit was a negative clamper)
V_{IN} = ± 3.5 V (given)

When input reaches -3.5 V, the -ve plate of the capacitor is -3.5 V and the positive plate of the capacitor is -0.3 V. Therefore, the voltage across capacitor is -3.5 V – (-0.3 V) = -3.2 V. Refer diagrams 2.92 and 2.93 below

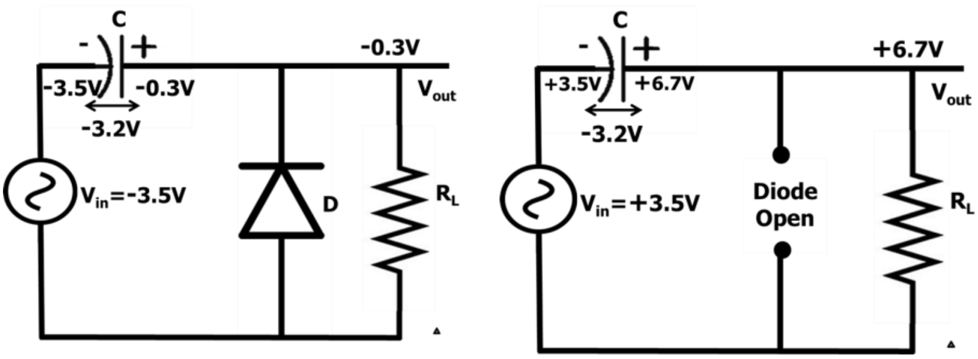


Fig 2.92

1) When V_{in} = -3.5 V
V_{out} = - 3.5 V – (- 3.2 V)
= - 3.5 V + 3.2 V
= - 0.3 V.
2) When V_{in} = 0 V
V_{out} = 0 v - (- 3.2 V)
= + 3.2 V
3) When V_{in} = +3.5 V
V_{out} = + 3.5 V - (- 3.2 V)
= 6.7 V
Therefore an input voltage of +3.5 V to –3.5 V is converted as –0.3 V to +6.7 V. The output is clamped by +3.2 V as shown in fig 2.93.

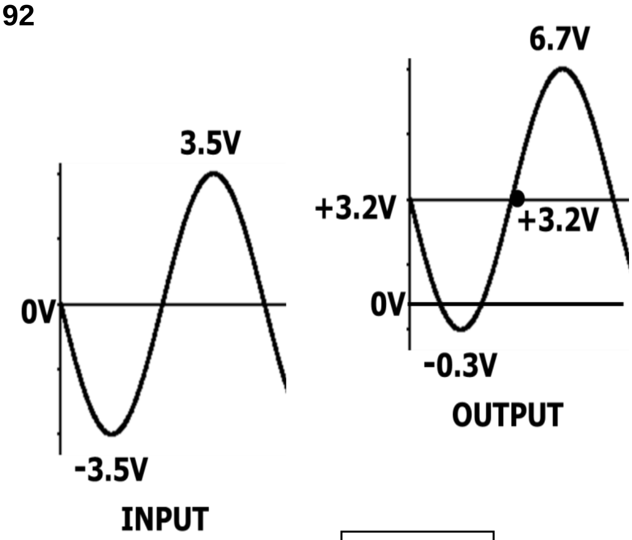


Fig 2.93

Problem 2.30: Biased clamper (silicon diode V_F = 0.7 V): Sketch input and output wave forms for this - ve clamper in fig 2.94.

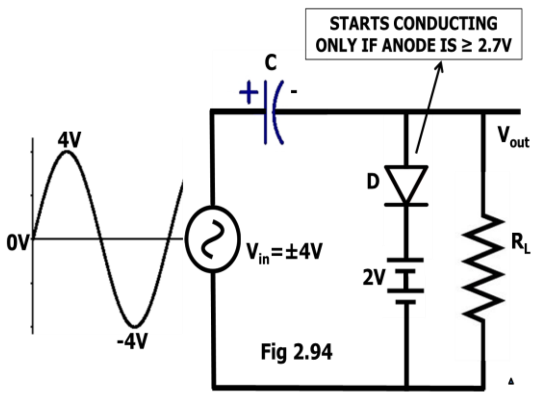


Fig 2.94

1) When does the diode conduct?
Cathode is at 2 V. Diode is Silicon. For the diode to conduct, anode needs to be 0.7 V more positive. than the cathode. Therefore diode starts conducting only if anode is ≥ 2.7 V.
2) What is the equivalent battery voltage of the capacitor?
Input (max peak) = +4 V
Diode starts conducting at 2.7 V
∴Voltage across the capacitor is 4 V – 2.7 V = +1.3 V.
This is the equivalent battery voltage.

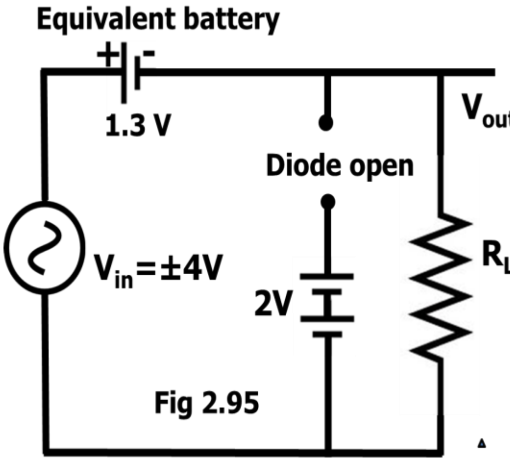


Fig 2.95

Input / Output waveforms: (Refer fig 2.95 and 2.96)

V_{out} = V_{in} - (1.3 V)

V_{in} = + 4 V; V_{out} = 4 V - 1.3 V = 2 .7 V

V_{in} = - 4 V; V_{out} = - 4 V - 1.3 V = -5.3 V

V_{in} = 0 V; V_{out} = 0 - 1.3 V = -1.3 V.

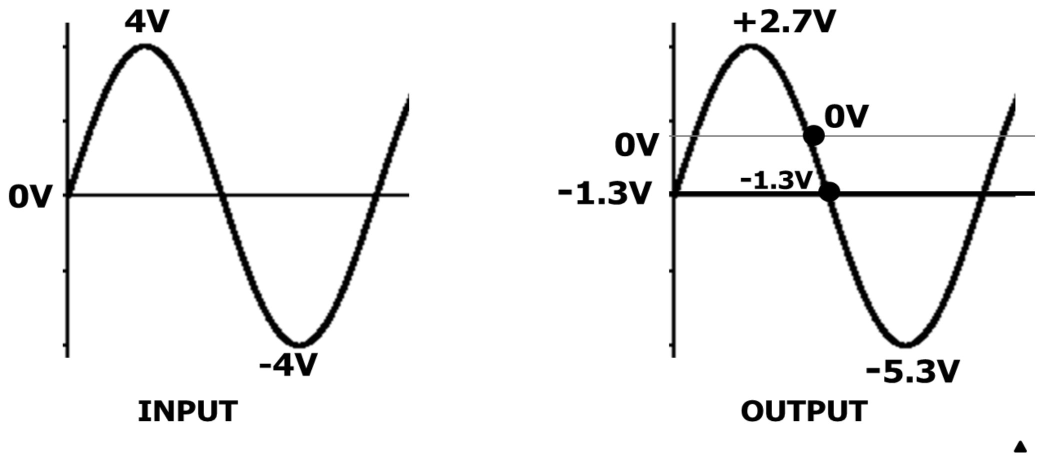


Fig 2.96

Numerical Problems

Problem 1: Design a Zener for an o/p of 5 V. Load current =10 mA, Zener Power = 400 mw, I/P voltage = 10 ± 2V.

Soln

$$\mathrm{R_L} = \frac{\mathrm{V_Z}}{\mathrm{I_L}} = \frac{5}{10 \times 10^3} = 500 \text{ ohms}$$
$$\mathrm{P_Z} = 400 \text{ mw}$$
$$\mathrm{I_Z} = \frac{\mathrm{P_Z}}{\mathrm{V_Z}} = \frac{400 \times 10^{-3}}{5} = 8 \text{ mA}$$
$$\mathrm{I_S} = \mathrm{I_Z} + \mathrm{I_L} = 80 + 10 = 90 \text{ mA}$$

Case 1 When input = 12 V (10 + 2)

R Series = $\frac{12-5}{90 \text{ mA}} = 77.77$ ohms

Case 2 When input = 8 V (10 - 2)

R Series = $\frac{8-5}{90 \text{ mA}} = 33.33$ ohms

Problem 2: A full wave rectifier supplies power to 1 k Ω load. The ac applied to the diodes is 300 V – 0 – 300 V. If the diode resistance is 25 Ω, find

(a) Average load current

(b) Average load voltage
(c) rms value of ripple voltage
(d) efficiency
Neglect transformer resistance.

Soln

300 V – 0 – 300 V is rms., R_f = 25 Ω, R_L = 1000 Ω

$$V_m = 300\sqrt{2} = 424 \text{ V}$$

$$I_m = \frac{V_m}{R_f + R_L} = \frac{424}{1000 + 25} = 0.414 \text{ A}$$

$$I_{dc} = {}^{2\,I_m}\!/_{\pi} = 0.263 \text{ A}$$

$$I_{rms} = {}^{I_m}\!/_{\sqrt{2}}$$

$$V_{dc} = I_{dc} \times R_L = 263 \text{ V}$$

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{{I_{dc}}^2\, R_L}{{I_{rms}}^2 (R_L + R_f)}$$

$$= \frac{\left(4\, {I_m}^2\, R_L/_{\pi^2}\right)}{\left({I_m}^2/_2\right)(R_L + R_f)}$$

$$= \frac{8}{\pi^2}\left(\frac{R_L}{R_f + R_L}\right) = 79.01\% \text{ (approx)}$$

Problem 3: An ac voltage of 25 V is connected in series with a silicon diode. The load resistance is 100 Ω. I_f = 10 Ω (Fwd resistance of diode) find, peak current through the diode and peak voltage thro R_L and V_{dc}

Soln

V_{rms} = 25 V, R_L = 1 K, R_f = 10 Ω

$$I_m = V_{rms} \times 2 = 50\text{V} \qquad \left(\text{in HWR}:\ \frac{V_m}{2} = V_{rms}\right)$$

$$V_m = \frac{V_m}{R_f + R_L} = 49.5 \text{ mA}$$

$$V_{dc} = \frac{V_m}{\pi} \cdot \frac{R_L}{R_f + R_L} = 15.71 \text{ mA}$$

Max outout across load = $I_m R_L$ = 49.5 V

Problem 4: Ideal diodes are used in a bridge rectifier. The source voltage is 230 V, 50 Hz. Load resistance is 200 ohms. Transformer turns ratio is 4 : 1. Find dc o/p voltage and frequency of output.

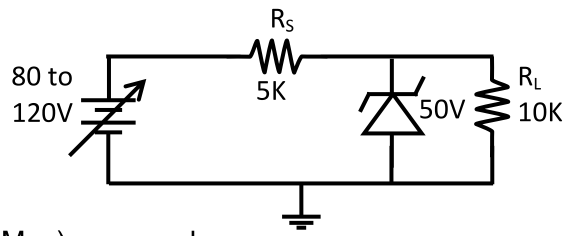
Freq of O/P in Bridge (Full-wave) rectifier = 2f = 100 Hz
V_{rms} = 230 V, R_L = 200 Ω, Turns ratio = 4 : 1
∴ I/P to Bridge diodes = 230 / 4 = 57.5 V (rms)

$$V_m = V_{rms} \times \sqrt{2} = 81.3\text{V.}$$

$$V_{dc} = \frac{2\,V_m}{\pi} = 52 \text{ V.}$$

$$P_{dc} = {I_{dc}}^2 \cdot R_L = \frac{(V_{dc})^2}{R_L} = \frac{52 \times 52}{200} = 13.2 \text{ W.}$$

Problem 5: For the circuit shown, fine max and min vale of Zener current.



Case 1

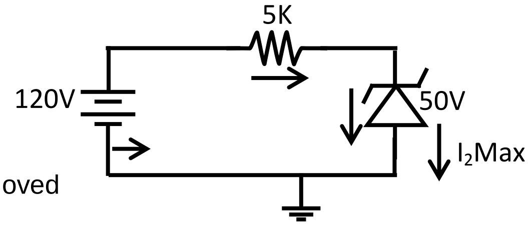
I_2 (Max) occurs when

(a) R_L is removed and

(b) V_{in} is maximum

$I_Z Max = \frac{120-50}{5K} = 14$ mA.

The entire current flows thro Zener since R_L is removed



Case 2

I_2 (Min) occurs when

(a) 10K is connected (R_L)

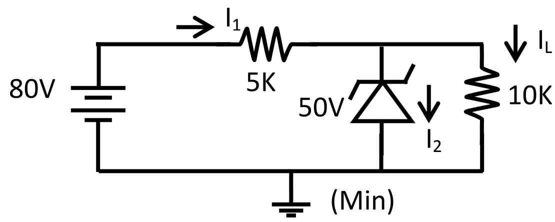
(b) V_{in} = Min = 80 V

since Zener voltage = 50 V, voltage across R_L also is 50 V

$I_L = \frac{50V}{10K} = 5$ mA.

$I_1 = \frac{80-50}{5K} = 6$ mA.

$\therefore$ I_Z min $= I_1 - I_L = 6 - 5 = 1$mA



Problem 6: A 24 V, 600 mw Zener diode is used to provide 24 V stabilized supply to a variable load. Input is 32 V. R_L = 1200 Ω.

Calculate

(1) The series resistance required.

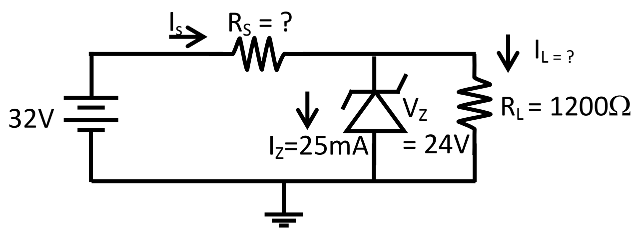
(2) Zener current when load = 1200 Ω

Soln :

P_Z = 600 mw, V_Z = 24 V. I_Z = ?

(a) $P_Z = V_Z \times I_Z$ $\quad \therefore I_Z = \frac{600 \text{ mw}}{24V} = 25$ mA

(b) I_L =? $\quad \frac{24 \text{ V}}{1200\,\Omega} = 20$ mA [since Zener voltage = 24 V, voltage across R_L also is 24 V]



(c) I_S = ? $\quad I_S = I_Z + I_L$ = 25 + 20 = 45 mA

(d) Rs = ? $\quad R_s = \frac{\text{Volage across } R_S}{\text{Current thro } R_S} = \frac{32 \text{ V} - 24 \text{ V}}{45 \text{ mA}} = \frac{8 \text{ V}}{45 \text{ mA}} = 177.78\,\Omega$

Problem 7: In a 2 diode full wave rectifier, the voltage across half the secondary is 100 V. Load Resistance is 950 Ω and R_f = 50 Ω . Find load current of RMS current.

V_{rms} = 100 V $\quad I_{dc}$ = ? $\quad I_{rms}$ =?

$$I_{rms} = \frac{V_{rms}}{R_L + R_f} = \frac{100}{950 + 50} = 100 \text{ mA}$$

$$V_m = V_{rms} \times \sqrt{2} = 100 \times 1.414 = 141.4 \text{ V}$$

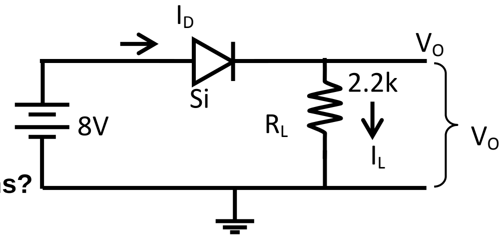
$$I_{dc} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi\,(R_L + R_f)} = \frac{2 \times 141.4}{\pi \times 1000} = 0.08998\text{ A} = 89.98\text{ mA}$$

Problem 8: What is V_O? What is the diode current?

The diode used is silicon, therefore V_f = 0.7 V

The voltage across RL = 8 — 0.7 V = 7.3 V

Current thro RL = Current ho diode = $\frac{7.3\text{ V}}{2.2\text{ K}} = 3.32\text{ mA}$



Problem 9: If the diode is reversed in example 8, what happens?

The diode is reverse biased,

There is no current flow anywhere

Output across R_L = 0 V.

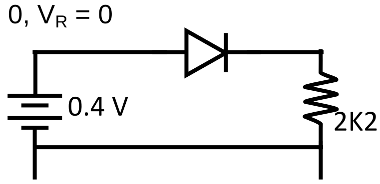
Current I_L = 0

Current I_D = 0

Problem 10: If the supply voltage is 0.4 V in example 8, what happens?

The diode is not sufficiently forward biased (silicon diode needs 0.7 V to conduct). Diode does not conduct

$\therefore$ I_L = 0, I_D = 0, V_R = 0



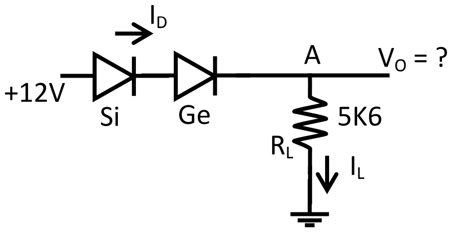
Problem 11: V_O = ? I_D = ?

Voltage at A = 12 V – Silicon Diode drop – Germanium diode drop

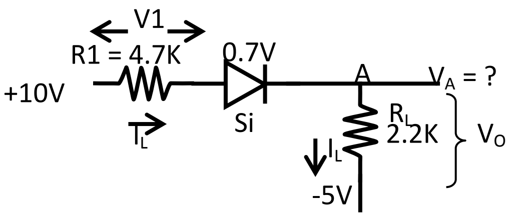
= 12 V – 0.7 V – 0.3 V = 11 V.

$I_L = \frac{11\text{ V}}{5600\Omega} = 1.96\text{ mA}$

I_D = I_L = 1.96 mA



1) V_A = ? V_O = ? I_L = ?



Method 1

KVL : Kirchoffs Voltage law

As per KVL : $-10\text{V} + (I_L \times 4.7\text{K}) + 0.7\text{V} + (I_L \times 2.2\text{K}) + 5\text{V} = 0$

I_L = 2.07 mA

$V_1 = I_L \times R_1$ = 2.07 mA x 4.7 K = 9.73 V (approx)

The DC Voltage at A = 10 – V1 – 0.7

= 10 – 9.73 – 0.7 = -0.43V.

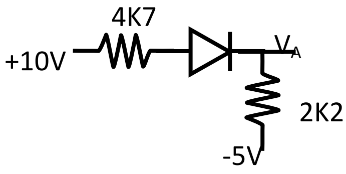
V_O = $I_L \times R_L$ = 2.07 mA x 2.2 K = 4.55 V (approx)

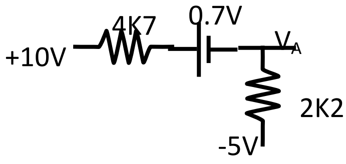
Method 2

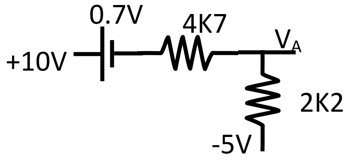
If you are not yet familiar with kirchoff's laws,

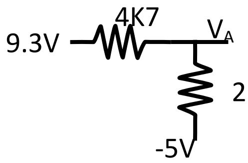
Draw equivalent circuit

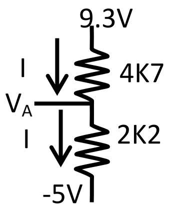
i)











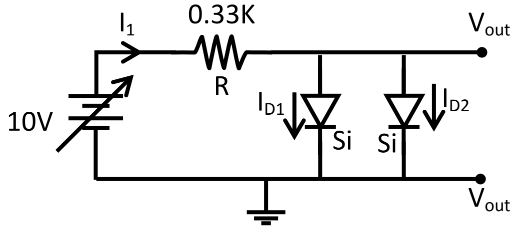
Total Current I = ?
Total Voltage = 9.3 V + 5 V = 14.3 V
Total Resistance = 4K7 + 2K2 = 6.9 K

$\therefore\ I = \frac{14.3\ V}{6.9\ K}$

Find I
Drop across 4K7 = I x 4.7 K
Drop across 2K2 = I x 2K2 & so on ………………

Problem 12: Analyze this circuit.

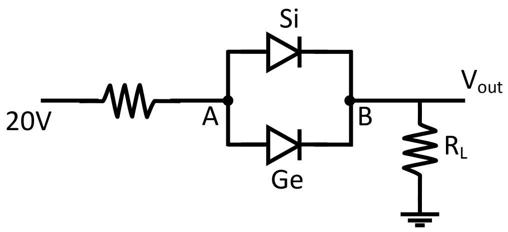
(a) I_1 = ? $\frac{10\ V - V_{out}}{0.33\ K}$
(b) V_{out} = ? V_{out} = 0.7 V (since both are silicon didoes with 0.7 V drop)



(a) $I_L = \frac{10 - 0.7\ V}{0.33\ K}$ = 28.18 mA

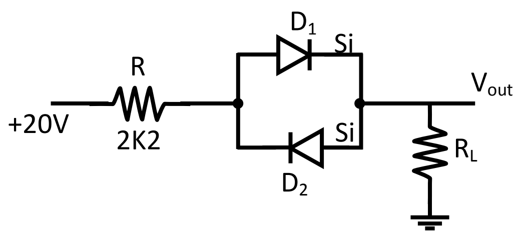
(b) What is ID1 & What is ID2?
I_1 is shared equally by diode 1 and diode 2
$\therefore\ I_{D1} = I_{D2} = I_1/2$ = 14.09 mA

Problem 13: What is V_{out}?



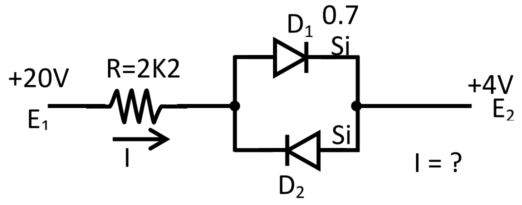
Across AB there are 2 diodes Si and Ge. When Germanium conducts V_{AB} will be frozen at 0.3V.
On the other hand Si diode requires 0.7 V to conduct, which it will never get. Therefore Si diode will never ever be able to conduct.
$\therefore$ Vout = 20 V – V_{ge} = 20 V – 0.3 V = 19.7 V

Problem 14: What is V_{out}?



If input is +20 V, D1 is FWD biased & will conduct. Diode D2 will always be reverse biased and will not conduct.
$\therefore\ V_{out}$ = 20 – 0.7 V = 19.3 V

Problem 15: What is I ?

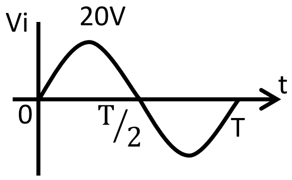


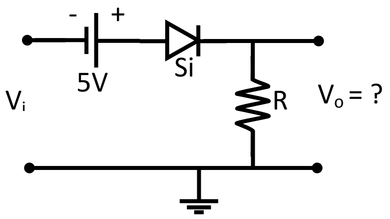
D1 - FWD biased & will conduct
D2 - REV biased & will NOT conduct

$$I = \frac{E_1 - E_2 - V_f}{R}$$

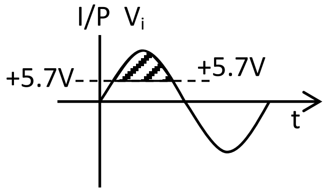
$$I = \frac{20\text{ V} - 4\text{ V} - 0.7\text{ V}}{2.2\text{ K}} = \frac{15.3\text{ V}}{2.2\text{ K}} = 6.95\text{ mA}$$

Problem 16: For the circuit shown, what is the o/p waveform?



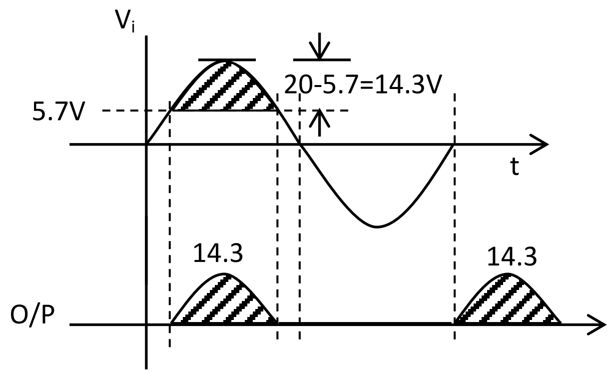


When Will the diode become forward biased ?



(a) Cathode is at 0 V
(b) Anode is at +5V (due to series Battery)
(c) $\therefore$ Diode will conduct ifand only if the input sine wave goes above +5.7V.
(d) $\therefore$ The o/p wave form will be that portion of Input Sine wave with amplitude > +5.7V as shown in fig (Hatched)

(e) The output will be zero when I/P is below +5.7V.



Chapter 3 Basics of Bipolar Junction Transistors

3.1 Transistor Introduction

What is a transistor?

- A transistor is a semiconductor device. It is a **3 layer device**. Two types of arrangements are possible -- **npn or pnp.**
- It has three layers **– emitter, base and collector**
- Transistor is a **current controlled** device and NOT a **voltage controlled** device.
- A very **small amount of current in the base region can control a large amount of current between emitter and collector**. This means transistor can be used in **current amplification** and therefore power amplification..
- Transistor can be used as a **basic switch (on–off switch) in digital logic circuits**

3.1.1 Transistor construction and circuit symbols:

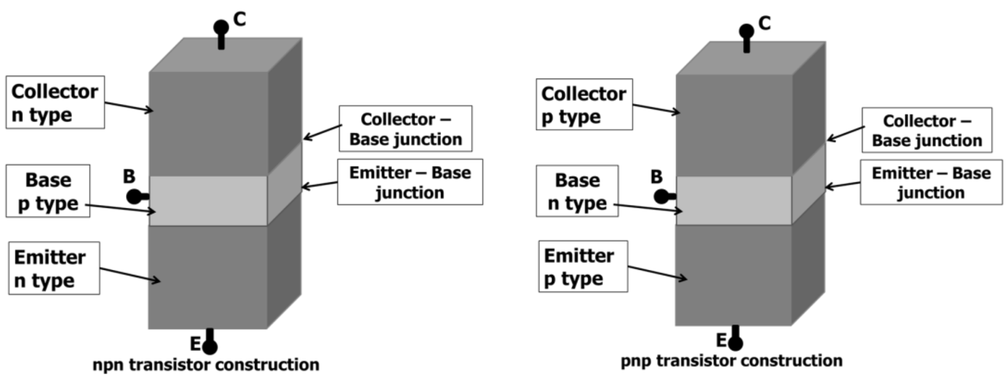


Fig 3.1

Figure 3.1 shows two types of transistor packages in semiconductor form – NPN and PNP.

PNP Transistor:

In PNP, **a n type semiconductor is sandwiched** between two p type semiconductors. The transistor has three terminals – **E**mitter (p type), **B**ase (n type) and **C**ollector (p type)

NPN Transistor:

In NPN, a **p type semiconductor is sandwiched** between two n type semiconductors. The transistor has three terminals – **E**mitter (n type), **B**ase (p type) and **C**ollector (n type)

Transistors have **two pn junctions, a collector base junction and an emitter base junction**.

3.1.2 Circuit Symbols:

The circuit symbols for an NPN transistor and a PNP transistor are shown in fig 3.2. The **emitter is always identified through an arrow**. The direction of the arrow indicates the direction of the current flow.

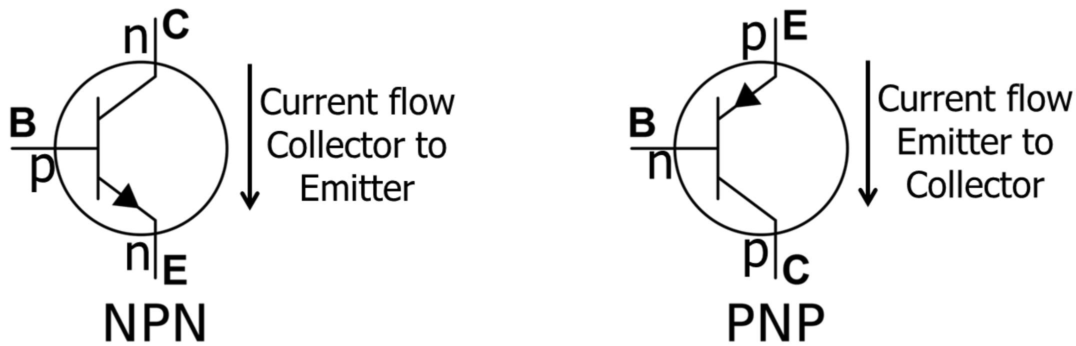
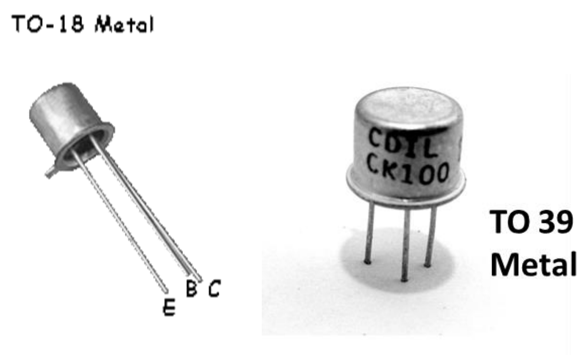


Fig 3.2



In a NPN transistor, the current is flowing out of the emitter and in a PNP transistor, the current is flowing into the emitter. The current flow direction also is indicated in the diagram.

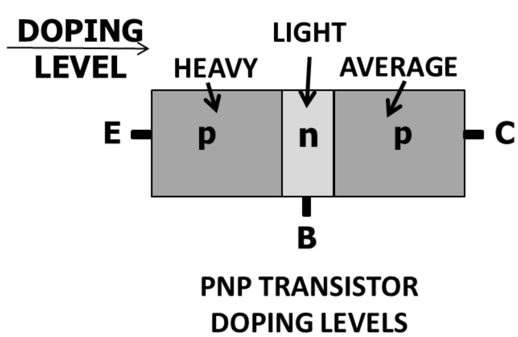
In NPN type the arrow is from p to n. In PNP type the arrow is also from p to n. Therefore remember that the current flow is always from p to n.

Fig 3.3

Some common metal can packages found in your lab are shown in fig 3.3

3.2 BJT Operation

3.2.1 pn junction operation



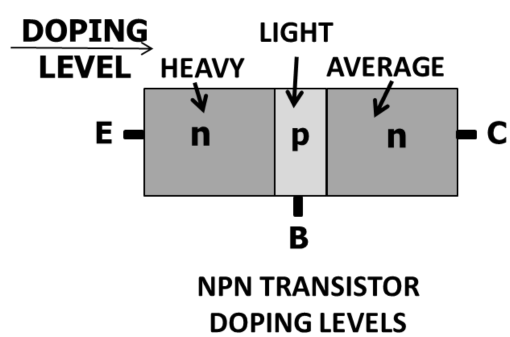


Fig 3.4 **Fig 3.5**

Recall the pn junction diffusion process discussed earlier on in section 1.4.1... The doping levels in emitter, base and collector are shown in fig 3.4 and 3.5

3.2.2 No bias: In the absence of any bias voltage, some electrons move from n region (majority carriers) to p and some holes move from p region (majority carriers) to n. This causes a buildup of +ve ions in n region and -ve ions in the p region causing a potential barrier. This barrier prevents further movement of carriers across the junction.

3.2.3 Forward bias (Emitter-Base junction): A npn transistor is shown in fig 3.6. Connect an external battery to the pn junction such that **p is connected to +ve and n is connected to the –ve**

terminal of the battery. Under this condition **the emitter base junction is said to be forward biased.**

When a pn junction is forward biased,

- o **Electrons (majority carriers) from n side** are attracted by the +ve potential in the p side and therefore **electrons start crossing the junction and land in p side**.
- o **Holes (majority carriers) from p side** are attracted by the -ve potential in the n side and therefore **holes start crossing the junction and land in p side**
- o Current flows in the pn junction from p to n under forward bias conditions
- o **Current flow is due to majority carriers under forward bias conditions.**

3.2.4 Reverse bias (Collector-Base junction): Connect an external battery to the pn junction such that **p is connected to -ve and n is connected to the +ve terminal of the battery.** Under this condition the **collector base junction is said to be reverse biased.**

Majority carriers

- o Electrons (majority carriers) from n side are repelled by the -ve potential in the p side and therefore electrons move away from the junction and remain in n side itself.
- o Holes (majority carriers) from p side are repelled by the +ve potential in the n side and therefore holes move away from the junction and remain in p side itself.

Minority carriers

- o However, holes (minority carriers) from n side will be attracted by the -ve potential in the p side and therefore **holes start crossing the junction and land in p side.**
- o Similarly electrons (minority carriers) from p side will be attracted by the +ve potential in the n side and therefore **electrons start crossing the junction and land in n side**.

Current flow due to majority carriers is not possible under reverse bias conditions but current flow due to minority carriers is a distinct possibility.

3.2.5 Transistor operation: NPN

The biasing arrangement for a NPN transistor is shown in figure 3.6

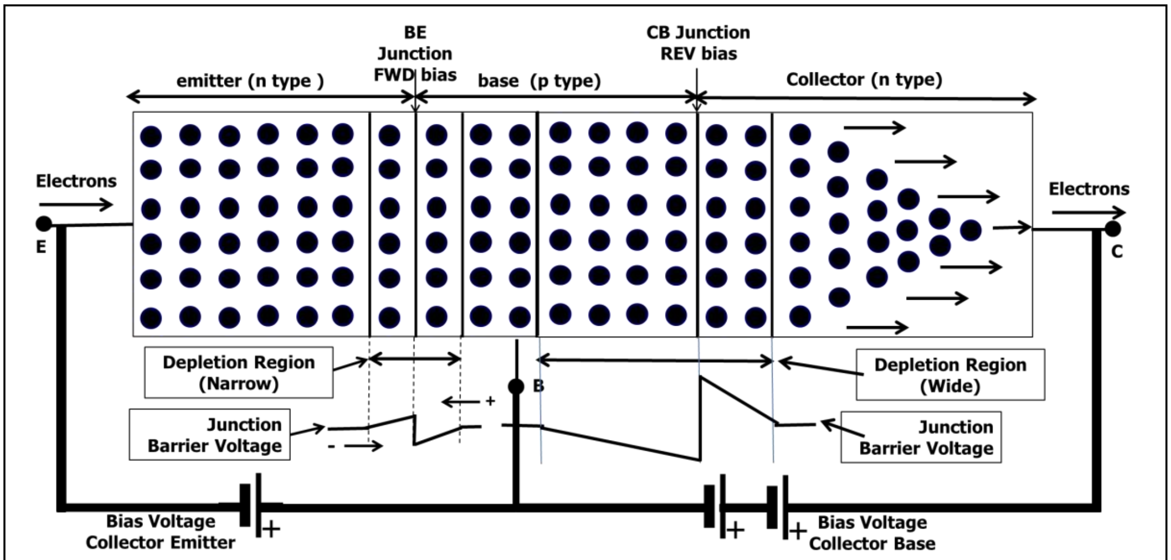


Fig 3.6 Semiconductor Physics of NPN Transistor

Recall:

- Fwd bias junction encourages flow of majority carriers

- Rev bias junction encourages flow of minority carriers
- In a transistor, **emitter and collector are heavily doped and the base is lightly doped. Base region also is very thin.**
- Emitter Base junction is forward biased. Emitter (n) is connected to –ve terminal of the battery and Base (p) is connected to +ve terminal of the battery.
- Current flow due to majority carriers happens. **Electrons from n region are emitted into the base (p) region.**
- This constitutes emitter current (I_E).
- Refer fig 3.7 here.
- **These emitted electrons are now in the base where they are minority carriers.**
- These electrons now see a **reverse bias between base (p) and collector (n). As we saw already, reverse base facilitates minority carrier flow and therefore these electrons are whisked away towards collector.**
- **The base is ultrathin and therefore almost all the electrons which were emitted by the emitter are collected by the collector. There is hardly any loss in the base due to recombination because base is lightly doped.**

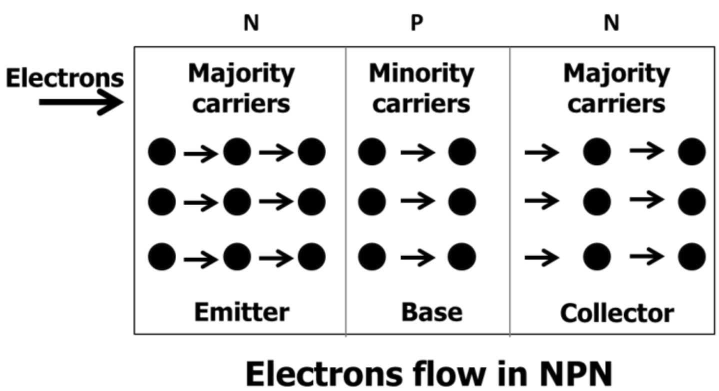


Fig 3.7

- **While the current flow discussion revolves around majority carriers (electrons), the minority carriers (holes) also are involved in the current flow. Therefore these devices are called bipolar junction transistors (BJT).**

3.2.6 Carriers flow in Transistors in npn

Refer fig 3.7.

- Electrons are the majority carriers
- Electrons from the emitter cross the Fwd Biased EB into Base.
- This constitutes emitter current (I_E)
- Majority of these Electrons (98 to 99%) transit thro base and through the rev biased CB into collector. This current is $I_C = 0.98\ I_E$
- That is why base width is kept small (for whisking away)
- Base doping is kept light so that recombination of holes and electrons is less probable. That is why base current is low and
- Very few holes cross from base to emitter

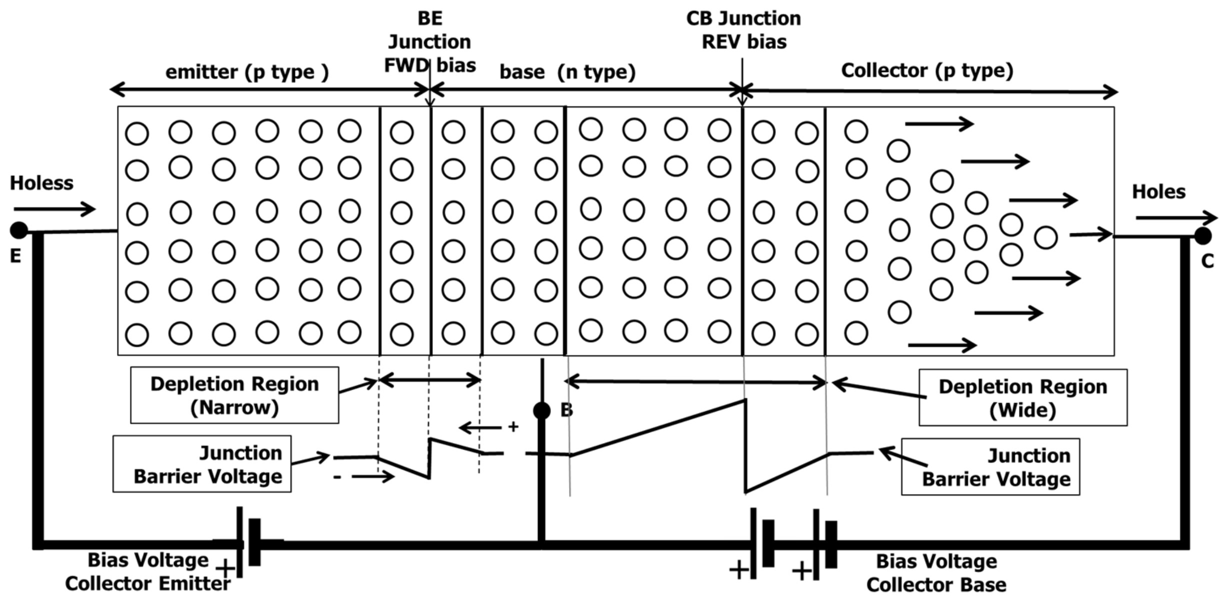
3.2.7 PNP transistor operation

Refer fig 3.8

The biasing arrangement for a NPN transistor is shown in figure

- Emitter Base junction is forward biased. Emitter (p) is connected to +ve terminal of the battery and Base (n) is connected to -ve terminal of the battery.

- These emitted holes are now in the base where they are minority carriers.
- These holes now see a reverse bias between base (p) and collector (n).
- As we saw already, reverse bias facilitates minority carrier flow and therefore these holes are whisked away towards collector.
- The base is ultrathin and therefore almost all the holes which were emitted by the emitter are collected by the collector.
- There is hardly any loss in the base due to recombination because base is lightly doped.
- While the current flow discussion revolves around majority carriers (holes) the minority
- carriers (electrons) also are involved in the current flow. Therefore these devices are called bipolar junction transistors (BJT).



Semiconductor Physics of PNP Transistor

Fig 3.8

3.2.8 Carriers flow in Transistors in pnp

- Holes are the majority carriers
- Holes from the emitter cross the Fwd Biased EB into Base.
- This constitutes emitter current (I_E)
- Majority of these holes (98 to 99%) transit thro base and through the rev biased CB into collector. This current is I_C. =0.98 I_E
- That is why base width is kept small (for whisking away)
- Base doping is kept light so that recombination of holes and electrons is less probable. That is why base current is low
- Very few electrons cross from base to emitter

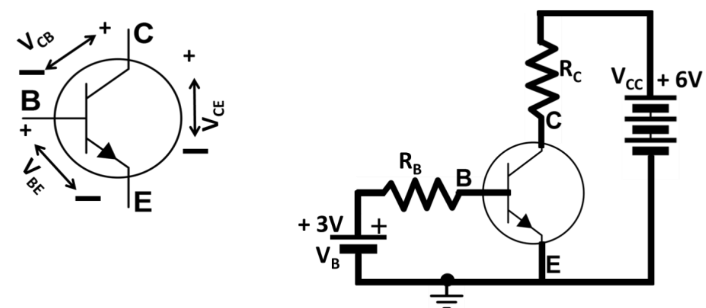
3.3 BJT Voltages and Currents (NPN)

3.3.1 Transistor Voltages:

The biasing arrangements for NPN transistor are shown in the figure 3.9

Base emitter junction : Must be forward biased. Base (p) must be more positive with respect to emitter (n). Note the battery polarity of V_B.

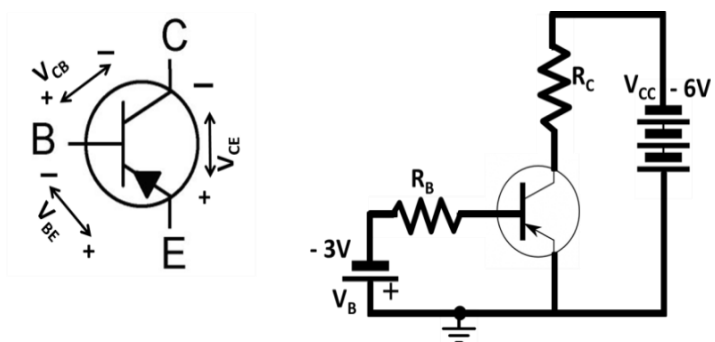
Base Collector junction : Must be reverse biased. Collector (n) must be more positive with respect to base (p) . Note the battery polarity of V_{CC}.



npn - polarity of terminal voltages

Fig 3.9

npn - power supply connections



pnp - polarity of terminal voltages

pnp - power supply connections

Fig 3.10

The biasing arrangements for PNP transistor are shown in the figure 3.10.

Base Emitter junction : Must be forward biased. Emitter (p) must be more positive with respect to base (n). Note the battery polarity of V_B.

Base Collector junction : Must be reverse biased. Collector (p) must be more negative with respect to base (n) . Note the battery polarity of V_{CC}

Biasing rules: Collector-base bias (V_{CC}) will always be greater than base bias V_{BB}. This ensures that the CB junction is always reverse biased. In our example, V_B= -3V and V_{cc}= -6V

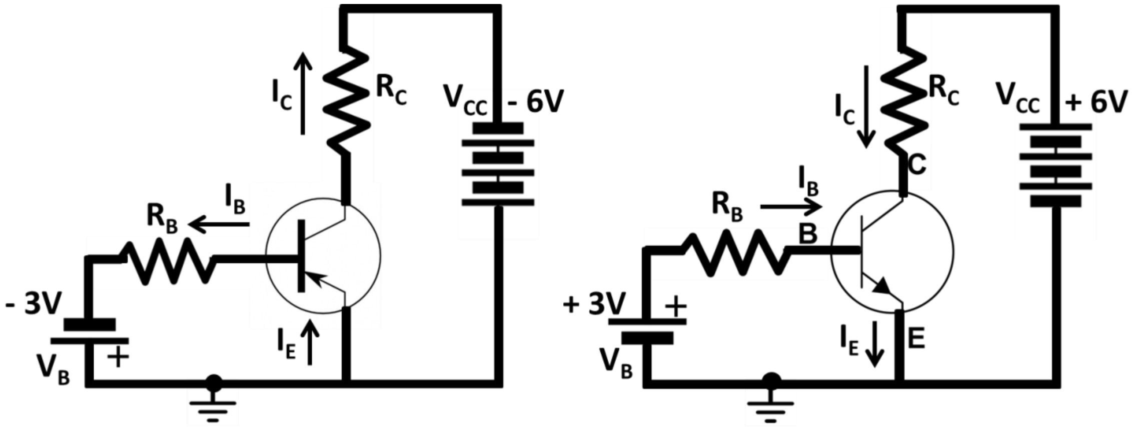
Current direction: Recall that the arrow indicates emitter and direction of the arrow indicates current flow direction.

.**Resistors R_B and R_C** are included in the circuit to limit the base current and collector current to safe limits.

Diode drops: Remember Base - Emitter Diode drop = 0.7V (Si) and 0.3 V (Ge)

3.3.3 Transistor currents:

The figure 3.11 shows the currents that flow in the transistor and the relationship between them.
For simplicity, the reverse currents are neglected for this analysis.



(a) pnp - current flow directions

Fig 3.11

npn - current flow directions

What are the different currents in a pnp BJT?

Refer fig 3.11(a). **I_E is the emitter current which flows into the transistor emitter.**
I_B and I_C are the currents that flow out of the transistor.

$I_E = I_B + I_C$

The entire current flow starts from the emitter. We had seen earlier that almost all the holes that originate from emitter reach collector and only a very few holes are lost in the base.

What are the different currents in a npn BJT?

Refer fig 3.11(b). I_C is the collector current which flows into the transistor. I_B is the base current which also flows into the transistor. I_E is the combined current, that flows out of the transistor.

$I_B + I_C = I_E$ 2.5-1

α_{dc} - Emitter to Collector DC current gain

The ratio of the collector current to the emitter current is defined as α. The typical value of α will be between 0.95 to 0.995 (very close to unity)

Emitter to collector DC current gain = $\alpha_{dc} = I_C / I_E$ 2.5-2

or $I_C = \alpha_{dc} I_E$ 2.5-3

α_{dc} is also known as common base current gain

$I_C = \alpha_{dc} (I_C + I_B)$ 2.5-4

Solving, $I_C = \dfrac{\alpha_{DC} \ I_B}{(1 - \alpha_{DC})}$ 2.5-5

β_{dc} - Base to Collector DC current gain (h_{FE})

β_{dc} is another important parameter of transistors. **It is defined as the ratio of collector current to base current. β_{dc} is also known as h_{FE}**

$\beta_{dc} = I_C / I_B$ 2.5-6

or $I_C = \beta_{dc} \ I_B$ 2.5-7

Relationship between α_{dc} and β_{dc}

(from 2.5-5) $\mathbf{I_C} = \dfrac{\alpha_{DC}\ I_B}{(1-\alpha_{DC})}$

$$\frac{I_C}{I_B} = \frac{\alpha_{DC}}{(1-\alpha_{DC})}$$

$$\beta_{dc} = \frac{\alpha_{DC}}{(1-\alpha_{DC})} \qquad 2.5\text{-}8$$

or $$\alpha_{dc} = \frac{\beta_{DC}}{(1+\beta_{DC})} \qquad 2.5\text{-}9$$

Problem 3. 1 : A transistor has a α_{dc} of 0.95. The base current is 0.015 mA. Find out I_B, I_C and β_{dc} ,

I_B = 0.015 mA = 150 μA. α_{dc} = 0.95

$\mathbf{I_C} = \dfrac{\alpha_{DC}\ I_B}{(1-\alpha_{DC})} = \dfrac{0.95 \text{ X } 150\ \mu A}{1-0.95}$ = 2.85 mA

$\mathbf{I_E = I_C / \alpha_{dc}}$ = 2.85 / 0.95 = 3 mA

$\beta_{dc} = \dfrac{\alpha_{DC}}{(1-\alpha_{DC})} = \dfrac{0.95}{1-0.95}$ =19

Problem 3. 2: A transistor has a collector current of 10 mA. The base current is 50 μA. Calculate I_E, β_{dc} and α_{dc} of this transistor. If the collector current doubles, what is the new emitter current?

β_{dc}	$= I_C / I_B$	= 10 mA/ 50 μA	= 200	
α_{dc}	$= \beta_{dc} /(1+ \beta_{dc})$	= 200 / (1+200)	= 200 / 201	= 0.995
I_E	$= I_B + I_C$	= 10 mA + 50 μA	= 10 mA + 0.05 mA	= 10.05 mA
	If collector current doubles, new I_C		= 20 mA	
New $I_B = I_C / \beta_{dc}$		= 20 mA / 200	= 100 μA	
New $I_E = I_B + I_C$		= 20 mA + 100 μA	= 20 mA + 0.1 mA	= 20.01 mA.

What is reverse leakage current (I_{CBO}) in transistor?

When the **collector-base diode** in a transistor semiconductor device is **reverse biased** ideally there should be nil current across the junction. However, due to increased barrier potential, the free electrons on the p side are attracted to the battery's positive potential and the holes on the n side are attracted to battery's negative potential. Thus the **minority carriers produce a very small reverse current** Hence it is also called as reverse saturation current **(I_{CBO})**.

Therefore ideally $\mathbf{I_C = \alpha_{dc} I_E + I_{CBO}}$

3.4 BJT Amplification

3.4.1 BJT Current Amplification

It is stressed here that the transistor is, a current amplifier.

The **DC current gain $\beta_{dc} = I_C / I_B$** . A small base current produces large collector current. This is a DC parameter. **A small amount of base current variation ΔI_B will produce a large amount of collector current variation as ΔIc.** Therefore

DC Current amplification = $\beta_{dc} = \Delta Ic / \Delta I_B$.

But, amplifiers work on ac mode. Therefore we can **define a new term $\beta_{ac} = I_c / I_b$.**
Convention **: Capital letters for DC parameters and small letters for ac parameters.**

3.4.2 BJT voltage Amplification

In a transistor amplifier,

1. Small variation in base current results in **small variations of base voltage**.
2. However, a small variation in base current results in large variations in collector current.
3. Large variation in collector current leads to **large variations of collector voltage**.

Correlate 1, 2 and 3. **Small variations in base voltage results in large variations in collector voltage. Therefore voltage amplification happens**

Voltage amplification = $\frac{\Delta V_C}{\Delta V_B}$

Conclusions:
Transistor produces current amplification and as a consequence voltage amplification too.

Problem 3.3: What is the voltage amplification of the circuit in fig 3.12?
<u>Base side:</u>
Base voltage variation = ΔV_B = ±30 mV. I_B = 16 μA
From the graph, base current variation = ΔI_B = ± 4 μA variation.

<u>Collector side :</u>
ß =100 (given)

Therefore $I_c = \beta_{dc} \times I_B$	= 100 X 16 μA = 1.6 mA.	
The voltage drop across R_c	= I_c X R_C	
	= 1.6 mA X 10K = 16 V	
Collector voltage (V_C)	= V_{CC} – voltage drop across R_c	
	= 25 V – 16 V = 9 V	
Collector current variation (ΔIc)	= ± 4 μA X 100	= ± 400 μA
Collector voltage swing (ΔVc)	= ΔIc X R_C	
	= ± 400 μA X 10000 ohms	= ± 4 V
Voltage amplification = ΔVc / ΔV_B	= ± 4 V / ± 30 mV	= 133.33

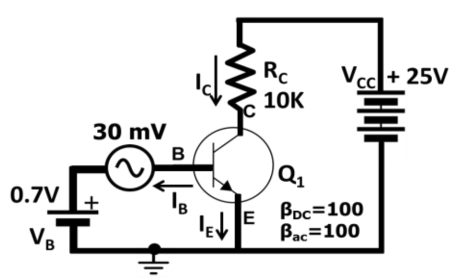
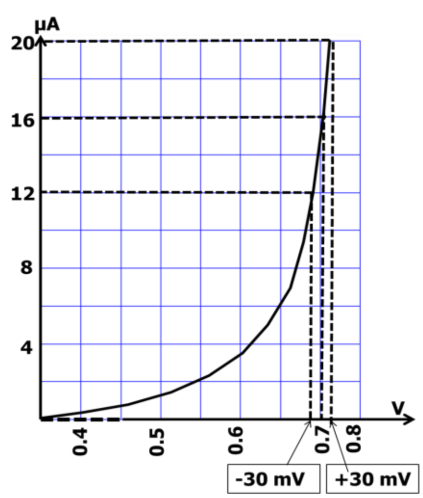
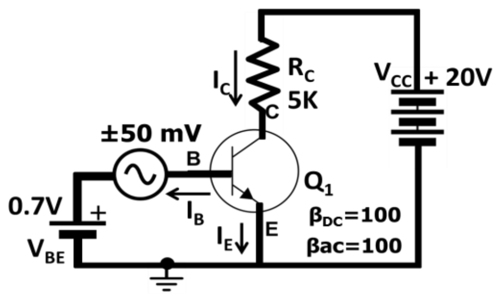


Fig 3.12



Problem 3.4: For the I_B vs V_{BE} characteristics in fig 3.13, what is the voltage gain?



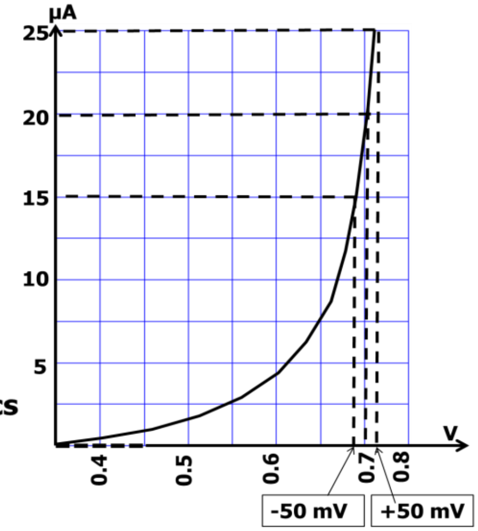


Fig 3.13 I_B vs V_{BE} characteristics

Base side:

Base voltage variation = ΔV_B = ± 50 mV, I_B = 20 μA

From the graph, base current variation = ΔI_B = ± 5 μA variation.

Collector side :

β_{dc} =100 (given), I_B = 20 μA,

Therefore $I_c = \beta_{dc} \times I_B$ = 100 X 20 μA = 2 mA.

The voltage drop across R_c = I_c X R_C

= 2 mA X 5K = 10 V

Collector voltage (V_C) = V_{CC} – voltage drop across R_c

= 20 V – 10 V = 10 V

Collector current variation (ΔIc) = ΔI_B X β_{ac}

= ± 5 μA X 100 = ± 500 μA

Collector voltage swing **:** ΔVc = ΔIc X R_C

= ± 500 μA X 5000 ohms (Since R_C = 5K)

= ± 2.5 V

Voltage amplification = $\Delta Vc / \Delta V_B$ = ± 2.5 V / ± 50 mV = 50

3.5 Common Base Characteristics

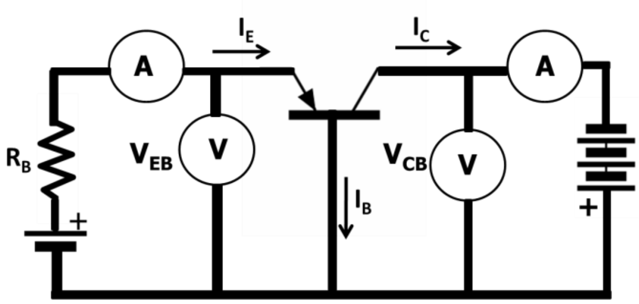


Fig 3.14 Test set up for measurement of Common Base Characteristics

Figure 3.14 shows a pnp transistor in common base configuration. **The base is common to both input and output terminals.**

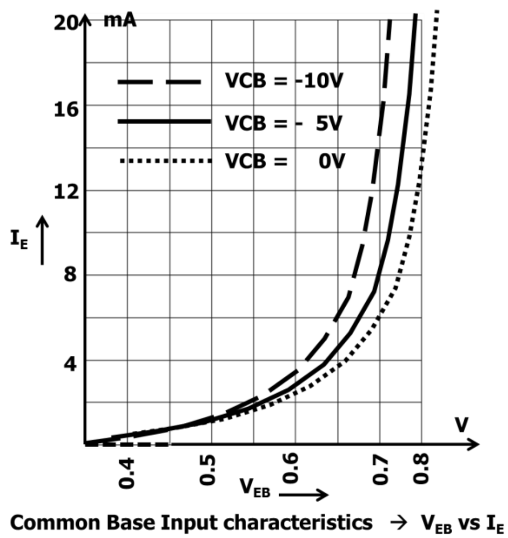
Common base characteristics deals with two analyses

- Study of input characteristics
- Study of output characteristics

Characteristics	X axis	Y axis	Variable
Input	V_{EB}	I_E	V_{CB}
Output	V_{CB}	I_C	I_E

3.5.1 Common Base Input Characteristics

Input characteristics are a plot of, input voltage (V_{EB}) in X axis and Input current (I_E) in Y axis, for various constant values of collector-base voltages.. It is similar to, a forward-biased diode characteristic.
The curve also shows that as the emitter base voltage is increased, emitter current increases.



Experiment.

1. Make the connections as per circuit in fig 3.14.
2. Keep V_{CB} at 0 V
3. Vary V_{EB} from 0.3 to 0.75 V & note I_E
4. Ensure V_{CB} does not vary
5. Plot the curve
6. Repeat 2 to 5 for other values of V_{CB}

Fig 3.15

3.5.2 Common Base output Characteristics

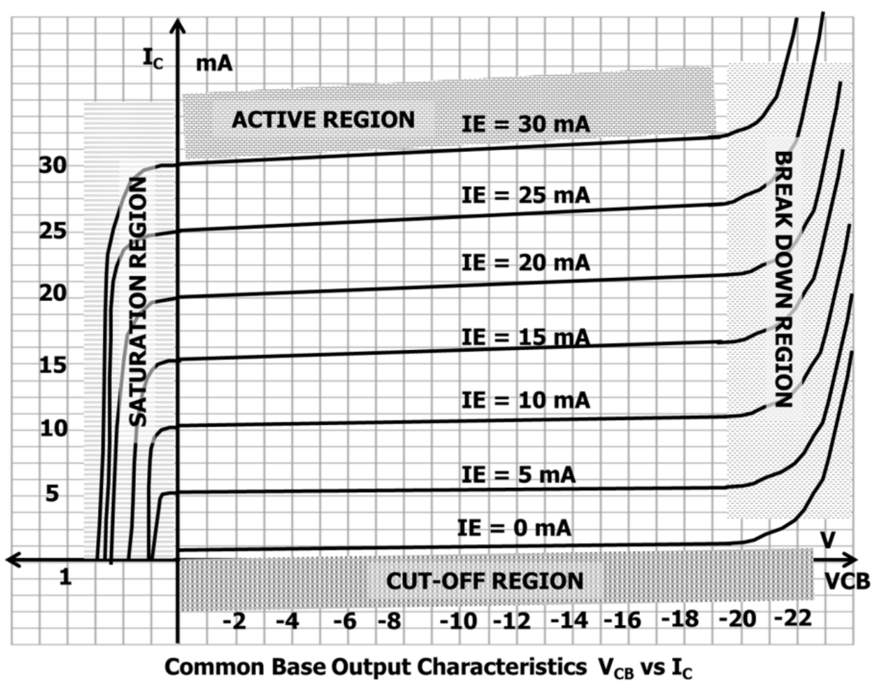


Fig 3.16

Experiment.

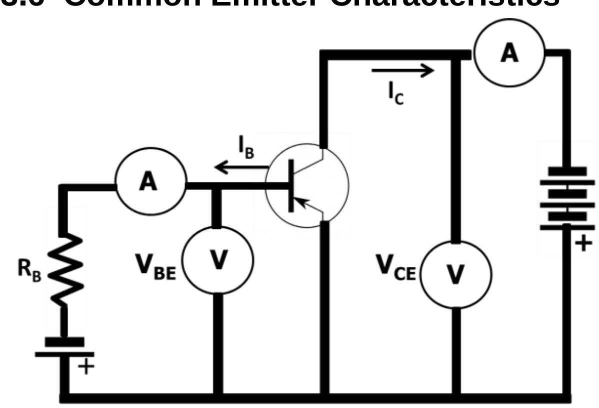
1. Make the connections as per circuit in fig 3.14.
2. Keep I_E at 1 mA.
3. Vary V_{CB} from 0 to -20 V for pnp (0 to +20 V for npn). Measure I_C
4. Ensure I_E does not vary.
5. Plot the curve.
6. Repeat 2 to 5 for other values of I_E.

Output characteristics is a plot of output voltage (V_{CB}) in X axis and output current (I_C) in Y axis, for various constant values of emitter currents.. The graph can be divided into four regions.

1. **Active region:**
   - **E-B junction forward bias. C-B junction reverse bias.**
   - In this region **collector current is almost equal to emitter current.**
   - Output current **(I_C) remains constant for a wide range of output voltage (V_{CB})**
2. **Saturation region:**
   - When output voltage **(V_{CB}) is zero, the output current (I_C) still flows**, mainly due to flow of minority carriers.
   - Output current **(I_C) becomes zero only when Collector base is forward biased**.
3. **Break down region:**
   - When **reverse bias increases beyond maximum permissible voltage, collector base junction breaks down.**
   - This is due to a condition known as **Punch Through** where collector-base depletion region penetrates too far into the base and meets emitter base depletion region.
4. **Cut-off region:**

The region below I_E=0, is known as cut off region. Transistor gets cut off. **Both collector base junction and emitter base junction are reverse biased**

3.6 Common Emitter Characteristics



Test set up for measurement of Common Emitter Characteristics

Fig 3.17

Figure 3.17, shows a pnp transistor in common emitter configuration. The emitter is common to both input and output terminals.

Common emitter characteristics deals with two analyses

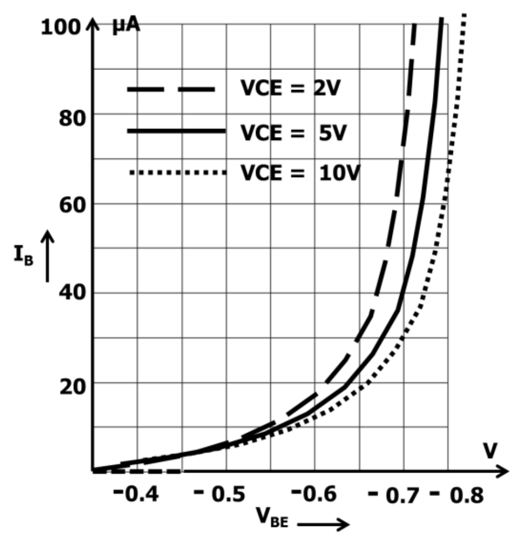
- Study of input characteristics
- Study of output characteristics

Characteristics	X axis	Y axis	Variable
Input	V_{BE}	I_B	V_{CE}
Output	V_{CE}	I_C	I_B

3.6.1 Common Emitter input Characteristics

Experiment.

1. Make the connections as per circuit in fig 3.17.
2. Keep V_{CE} at 2 V
3. Vary V_{BE} from 0.3 to 0.75 V and note I_B
4. Ensure V_{CE} does not vary
5. Plot the curve
6. Repeat 2 to 5 for other values of V_{CE}



Common emitter Input characteristics → V_{BE} vs I_B

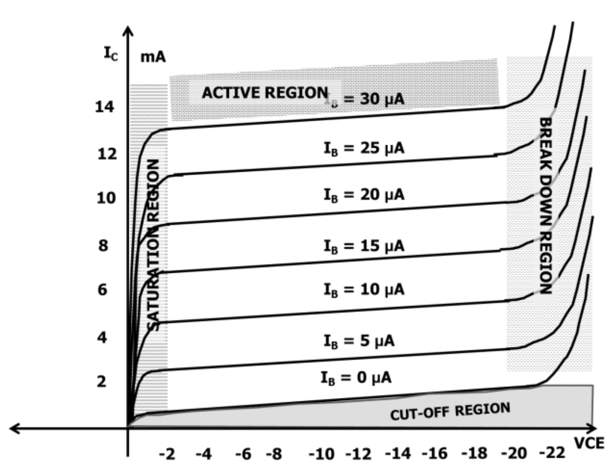
Fig 3.18

- Input characteristics (fig 3.18) is a plot of input voltage (V_{BE}) in X axis and Input current (I_B) in Y axis, for various constant values of collector-emitter voltages. It is also similar to a forward-biased diode characteristic
- The curve also shows that as the base emitter voltage is increased, base current increases beyond the knee voltage. **(Knee voltage is 0.7V for silicon and 0.3V for Germanium).**
- I_B reduces as V_{CE} is increased.

3.6.2 Common Emitter output Characteristics:

1. Make the connections as per circuit in fig 3.17.
2. Keep I_B at 0 μA
3. Vary V_{CE} from 0 to -20V for pnp (0 to +20V for npn). Measure I_C
4. Ensure I_B does not vary
5. Plot the curve
6. Repeat 2 to 5 for other values of I_B

Output characteristics (fig 3.19) is a plot of output voltage (V_{CE}) in X axis and output current (I_C) in Y axis. The graph can be divided into four regions



Common Emitter Output Characteristics V_{CE} vs I_C

Fig 3.19

1. **Active region:**
   - **E-B junction forward bias. C-B junction reverse bias.**
   - In this region output current (I_C) increases gradually, as output voltage (V_{CE}) increases.
   - This is the linear region suitable for amplifiers.

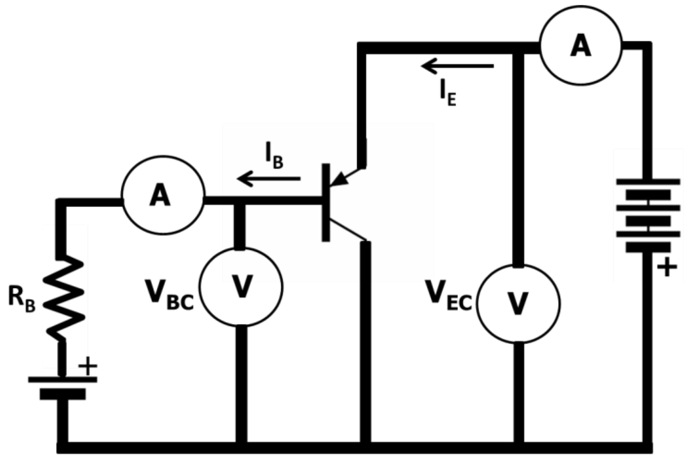
2. **Saturation region:**
   - **E-B junction forward bias. C-B junction forward bias.**
   - When output voltage (V_{CE}) is zero, the output current (I_C) is zero.
   - **V_{CE} at saturation is 0.3V for Silicon and 0.1V for Germanium**

3. **Break down region:**

- When reverse bias increases beyond maximum permissible voltage, collector base junction breaks down.
- This is due to a condition known as Punch Through where collector-base depletion region penetrates too far into the base and meets emitter base depletion region.

4. **Cut-off region:**

- The region below I_B=0 is known as cut off region. Transistor gets cut off. **Both collector base junction and emitter base junction are reverse biased**



Test set up for measurement of Common Collector Characteristics

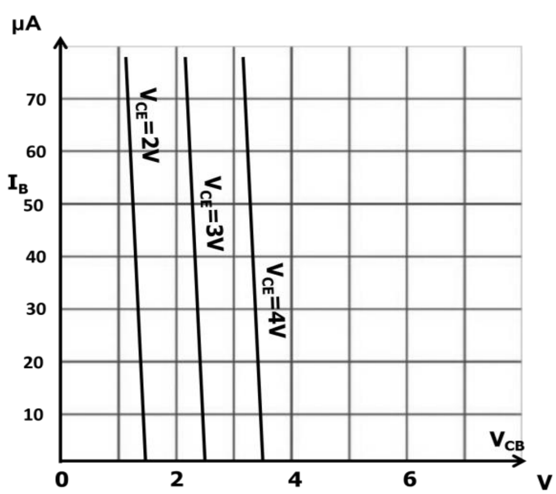
Fig 3.20

3.7 Common Collector Characteristics

Common collector amplifier is also known as **emitter follower. Refer fig 3.21**

Difficult to set up this experiment since I_B is very sensitive and keeps changing

3.7.1 Common Collector Input Characteristics



Common Collector Input Characteristics

Fig 3.21

Input characteristics in fig 3.21, is a plot of input voltage (V_{CB}) in X axis and Input current (I_B) in Y axis, for various constant values of collector-emitter voltages.

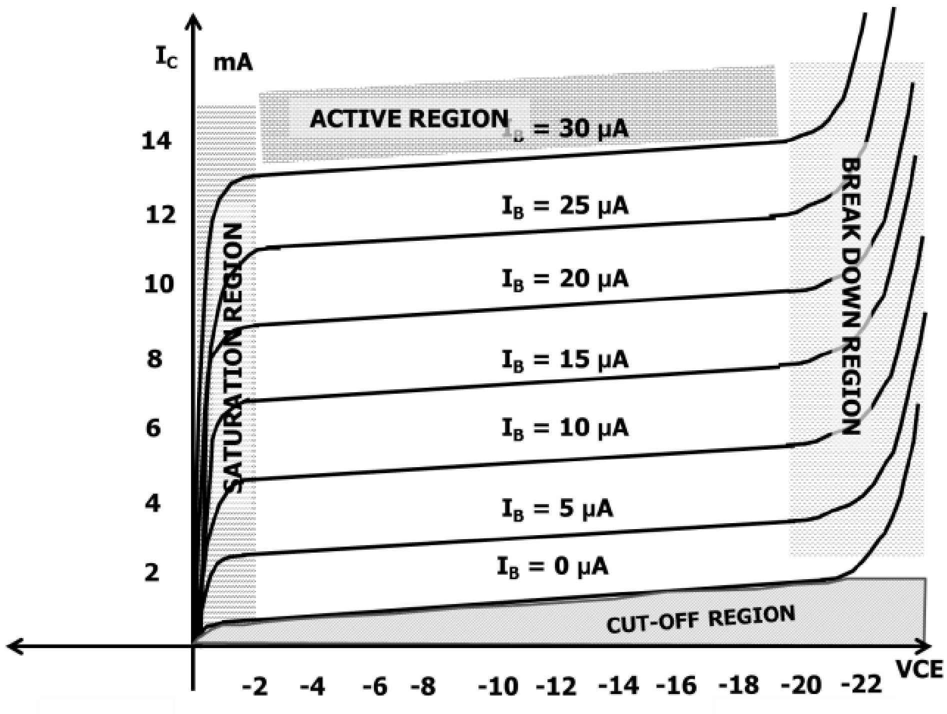
The characteristic exhibits a different behaviour than CB or CE configuration.

BC Junction (input) is fwd biased and CE Junction (output) is reverse biased.

We can see $\quad$ $\mathbf{V_{CE} = V_{CB} + V_{BE}}$

$\mathbf{V_{CB} = V_{CE} - V_{BE}}$

3.7.2 Common collector Output characteristics: Refer fig 3.22 . It is very much similar to Common emitter output characteristics in all respects



Common Emitter Output Characteristics V_{CE} vs I_C

Fig 3.22

Chapter 4: BJTs and FETs

Syllabus: BJT Biasing (Text-1) : DC Load line and Bias Point, Base Bias, Voltage divider Bias, Numerical examples as applicable.

4.1 Design Introduction

What are the design issues in transistor biasing?

- DC voltages of C,B and E **should be stable** and constant
- DC currents I_C, I_B and I_E **should be stable** and constant

What is a Q point?

Q point is known as **DC operating point or quiescent point**. It specifies the operating point of a transistor based on its circuit design. It is specified in terms of the value of **I_C and V_{CE} , with no input signal applied.**

- DC operating point or a **Q point always needs to be specified** for a transistor circuit.

Can a bias voltage or bias current remain constant? No. Why?

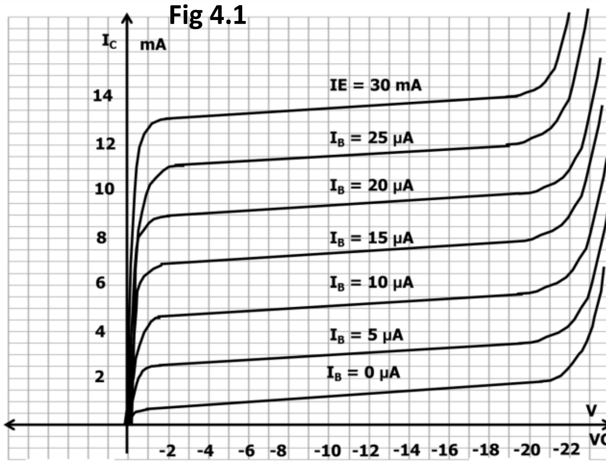
- **β (h_{FE}) variations and temp variations result in bias variations**

If the bias voltage can be made stable, Q point can be stabilized and designs can exhibit predictable behaviour.

What is a load line?

- **Load line is a straight line drawn on, BJT output characteristics (**Refer fig 4.1**)**
- Recall BJT O/P characteristics is a graph, with **V_{CE} on the x axis and I_C** on the y axis
- **Therefore any point on the load line, has coordinates (V_{CE}, I_C)**

Fig 4.1



Common Emitter Output Characteristics V_{CE} vs I_C

What is a load line for Common Emitter circuit?

It is a graph of **I_C vs V_{CE} (R_C and V_{CC} fixed)**

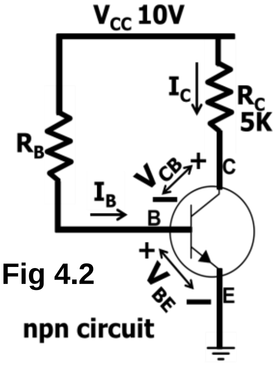


Fig 4.2

npn circuit

Why load line?

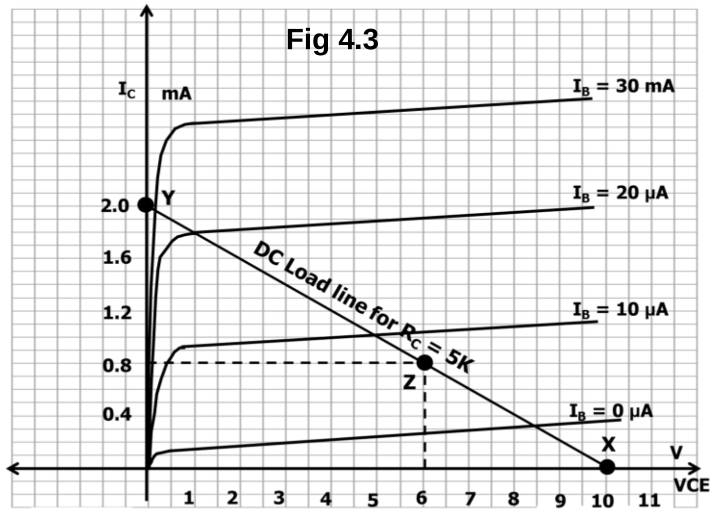
Load line gives a **complete analysis of all Q points** possible in a transistor circuit.

What is biasing and what are the biasing issues?

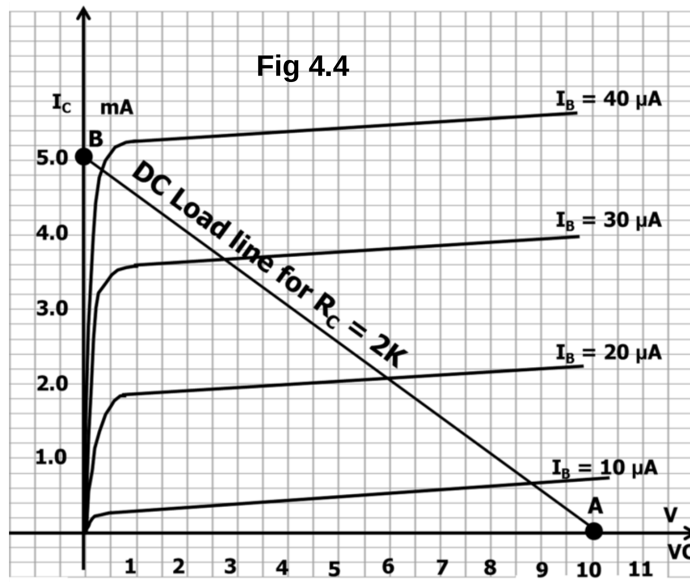
Look at fig.4.2. In the circuit, BE Junction is

forward biased and CB junction is reverse biased.

- For a transistor to operate as per design, **external DC voltages (V_{CC} Power supply) need to be applied**. The voltages should be of the **correct polarity and permissible magnitude for EB junction and CB junction**. This is known as **biasing**
- Emitter Base junction needs to be forward biased and Collector Base junction needs to be reverse biased. (0.7V for silicon or 0.3 V for gemanium need to be ensured)
- **The operating point of a transistor, has to be preferably at the center (V_{CE} = V_{CC}/2),** for maximum voltage swing on either side.
- The bias needs to be stabilised. The bias point should not vary due to temperature variations or β variations or input mains supply variations



Common Emitter Output Characteristics V_{CE} vs I_C



Common Emitter Output Characteristics V_{CE} vs I_C

What are the basic biasing techniques?

Three popular methods are used. They are**, Base bias, Collector to Base bias and Voltage Divider bias**.

4,2 DC Load line and Bias point

Problem 4.1: Draw a DC load line for the circuit shown in fig 4.2 for a V_{CC} =10 V

V_{CE} = V_{CC} – Voltage drop across R_C

= $V_{CC} – I_C R_C$

When V_{BE} = 0 V,

Transistor does not conduct. $I_C = 0$

V_{CE} = 10 V – (0 mA X 5 K ohm)

= 10 V.

Refer fig 4.3. Mark point X = 10 V on the X axis

When V_{BE} = 0.7 V

Transistor conducts. V_{CE} becomes zero

0 = 10 V – (I_C X 5 K ohm).

I_C = 2 mA. Mark point Y = (0 V, 2 mA) on the Y axis.

Recall, any point on the load line has the coordinates (V_{CE}, I_C). Join XY and this line is the DC load line for this circuit. If any one of these circuit parameters vary, a new load line is to be drawn.

What is the Q point at Z in fig 4.3?
I_C= 0.8 mA and V_{CE} = 6 V

Problem 4.2: Draw the new DC load line for the circuit in fig 4.2, when R_C = 2K
$V_{CE} = V_{CC} – I_C \times R_C$

Case1 :
V_{BE} =0, BJT → Not conducting, I_C = 0
V_{CE} = 10 V – 0 mA X 2 K = 10 V
Point A on load line will be (10 V, 0 mA)

Case 2:
V_{CE} = 0 V
0V = 10V – I_C X 2 K $\therefore I_C$ = 5 mA

Point B on load line will be (0V, 5 mA)
Draw AB…….This is the load line **for THIS circuit**.

4.2.1 Q point (quiescent point) of a transistor
What is a Q point of a transistor?
It is the DC Point of the transistor in a given circuit**. It describes its operating point, in terms of (VCE, IC) coordinates.** Ref fig 4.5 which is basically same as fig 4.4.

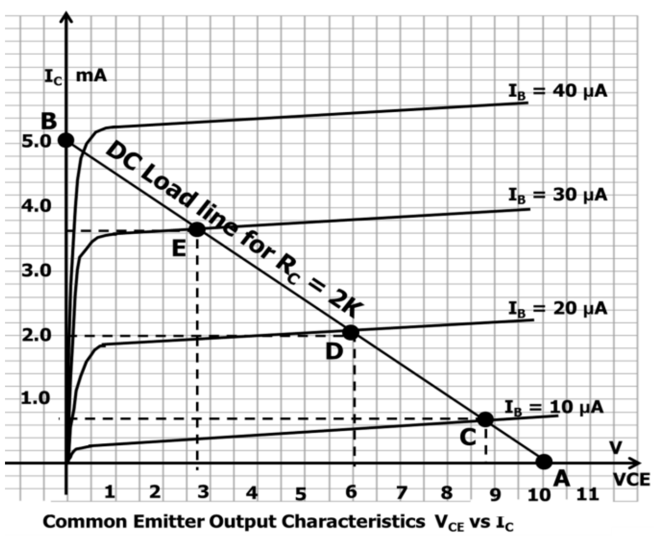


Fig 4.5

Q points analysis			
Q point	I_B (μA)	V_{CE} (V)	I_C (mA)
A	0	10	0
B	xx	0	5
C	10	8.8	0.7
D	20	6.0.	2.0.
E	30	2.7	3.6

Fig 4.6

Graph illustrates the relationship between the various Q points and **how they are related to the important circuit parameters such as I_B, I_C and V_{CE}**

The excel table (fig 4.6) tabulates five Q points (A, B, C, D, E) in the graph, in terms of these parameters.

4.2.2 What are the inferences?

1. When base current varies between 10 µA and 30 µA, V_{CE} varies between 2.7 V and 8.8 V.
2. At extreme points (A and B), the V_{CE} Swings between V_{cc} and 0 V.
3. The best Q point should preferably be, therefore at $V_{CC}/2$
4. The collector current varies between 5.0 mA (saturation) and 0 mA (cut-off).
5. Small variations in base current (10 µA to 30 µA) causes large variations in V_{CE} (2.7 V to 8.8 V)
6. Small variations in base current (10 µA to 30 µA) causes large variations in collector current I_C (0.7 mA to 3.6 mA). **<u>Transistor is a current amplifier</u>**

4.2.3 Q point – 2 conditions

This figure 4.7 illustrates two extremes of the Q point variations and the end points of the DC load line.

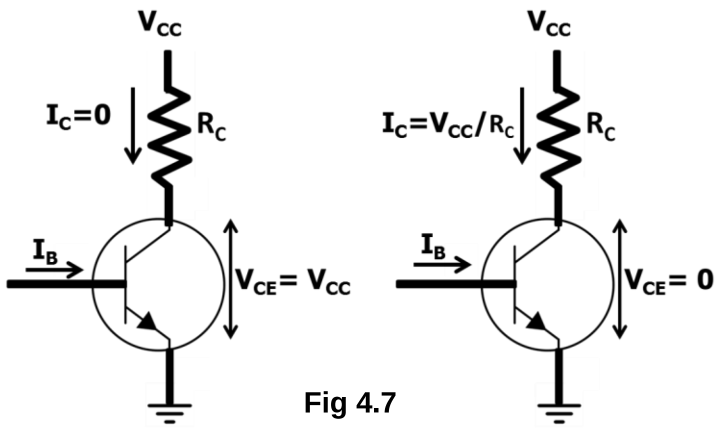


Fig 4.7

Q Point extremes (useful for drawing the load line)
(a) when I_C=0, V_{CE}= V_{CC}, (b)when V_{CE}= 0, I_C=V_{CC}/R_C

4.3 Base Bias

Problem 4.3: What is the Q point for this Germanium transistor in fig 4.8 ? Draw the DC load line. (β =100.)

V_{BE} = 0.3V (Germanium)

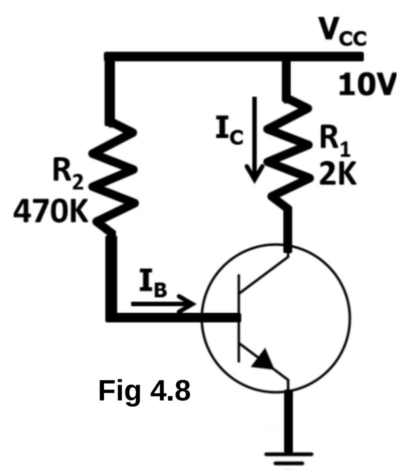


Fig 4.8

base bias

(a) Find I_B

Apply KVL

$V_{CC} – (I_B \times R_2) – V_{BE} = 0$

$10V – (I_B \times 470\ K) - 0.3\ V = 0$

$\therefore I_B$ = 20.6 mA

(b) Find I_c

$I_C = \beta \times I_B$ = 20.6 mA X 100 = **2.1 mA (Q point: I_C)**

(c) Find collector voltage V_c

$V_{CE} = V_{cc} - (I_C \times R_1)$

$= 10\ V - (2.1\ mA \times 2000\ \Omega)$

= **5.8 V (Q point : VCE)**

Therefore, Q point is **(5.8 V , 2.1 mA)**

(d) How to draw load line?

Point A : When $I_c = 0$, $V_{CE} = V_{CC} = 10V$, **A = (10 , 0)**

Point B : when $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_2} = \frac{10\ V}{2K}$ = 5 mA, **B = (0 , 5)**

Draw AB. The load line is shown in fig 4.9. Q point, as calculated = (5.8 V , 2.1 mA)

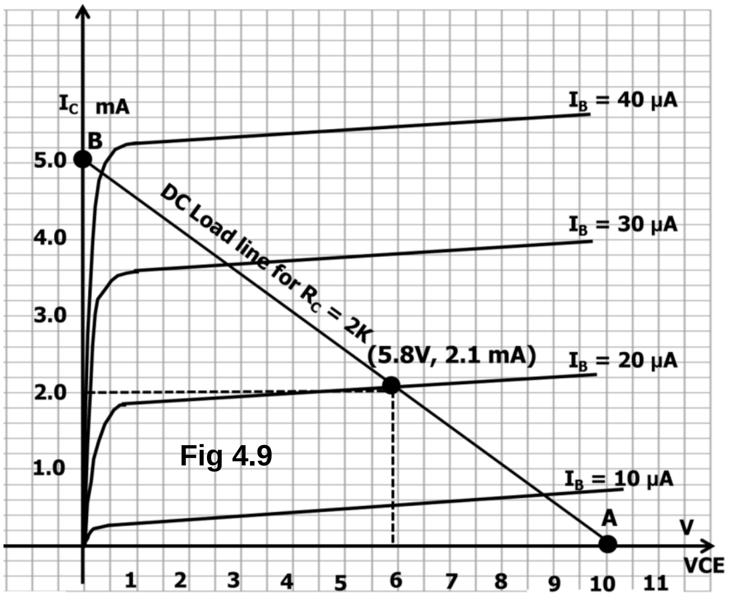


Fig 4.9

Q point (5.8V, 2.1 mA)

Problem 4.4: What is the Q point of this circuit in fig 4.10 and what is the emitter current? Assume silicon transistor.

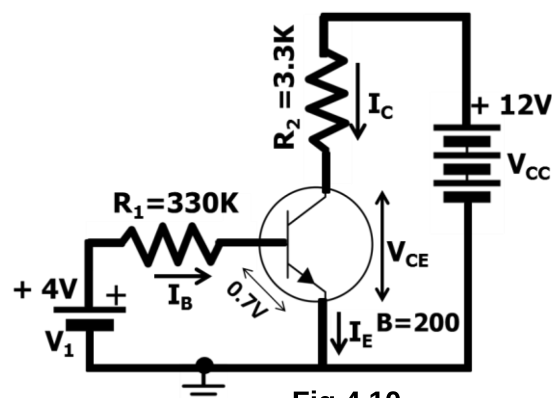


Fig 4.10

V_{BE} = 0.7 V (Si)

(a) **Base current**

$V_1 - (I_B \times R1) - 0.7\ V = 0$

$4V - (I_B \times 330\ K) - 0.7 = 0$

$I_B = \frac{3.3\ V}{330\ K}$ = **10 µA**

b) Collector current (I_C)

$I_C = I_B \times \beta$ = 10 µA X 200 = 2 mA

(c) V_{CE}

$V_{CE} = V_{CC} - I_C \times R2$

= 12 V –2 mA X 3300 Ω

= **5.4 V**

∴Q point = (V_{CE} , I_C) = (5.4 V, 2 mA)

(d) Emitter current

$I_E = I_B + I_C$ = 2 mA + 10 mA = 2.01 mA.

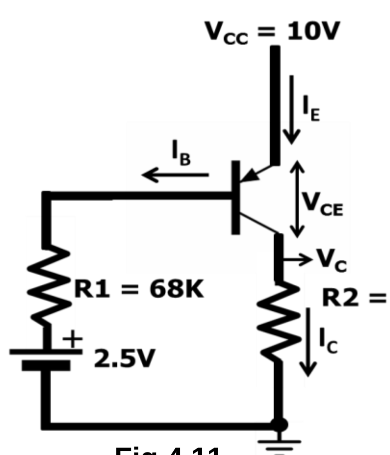


Fig 4.11

Problem 4.5: Look at the pnp. Silicon transistor in fig 4.11. β=100. Find all the currents and value of R2, given the condition $V_{EC} = \frac{V_{CC}}{2}$

(a) Find I_B

V_{EB} = 0.7 V (Silicon)

$V_B = V_{CC} - V_{EB} = 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$

Voltage across R1 $= 9.3\text{ V} - 2.5\text{ V} = 6.8\text{ V}$

$\therefore I_B = \frac{6.8\text{ V}}{68\text{K}} = 100\ \mu A$

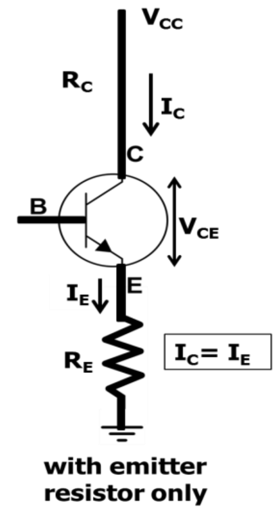


Fig 4.12

(b) Find I_C

$I_C = I_B \times \beta$

$= 100\ \mu A \times 100 = 10\text{ mA}.$

(c) Find R2

$V_{CC} = 10\text{ V},$

$V_{EC} = \frac{V_{CC}}{2}$ (given) $= \frac{10\text{ V}}{2} = 5\text{ V}$

V_C (at collector) $= 10\text{ V} - 5\text{ V} = 5\text{ V}$

$R2 = \frac{V_C}{I_C} = \frac{5\text{ V}}{10\text{ mA}} = 500\ \Omega$

d) Emitter current

$\mathbf{I_E = I_C + I_B}$

$= 10\text{ mA} + 100\ \mu A$

$= 10.1\text{ mA}$

4.3.1 Effect of emitter resistor

Look at this circuit. fig 4.12.

There is no resistor in the collector but there is an emitter resistor R_E. **What is the dc load line (R_L), for this circuit ?**

Let I_E be the emitter current

Applying KVL, $V_{CC} - V_{CE} - I_E R_E = 0$

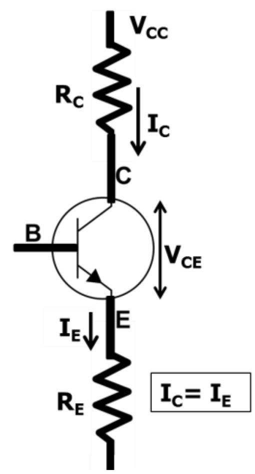


Fig 4.13

<u>Load line for this circuit</u>

Point B : When $V_{CE} = 0$, $\mathbf{I_E = \frac{V_{CC}}{R_E}}$

Point A : When $I_E = 0$, $V_{cc} = V_{CE}$

Look at this circuit fig 4.13.

There are two resistors, R_C and R_E .

What will be the dc load line (R_L) for this circuit?

For this circuit, the total dc load resistance = $\mathbf{R_c + R_E}$.

We need to make an assumption that **$I_C = I_E$ (neglecting base current)**

Applying KVL , $V_{CC} - I_C R_C - V_{CE} - I_c R_E = 0$

<u>Load line for this circuit</u>

Point A : When $I_C = 0$, $V_{CC} = V_{CE}$

Point B : When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C + R_E}$

Problem 4.6: Draw DC load line for this circuit in fig 4.14. What is the Q point ? Assume Germanium transistor, and assume β = 99. Find the Q point also.

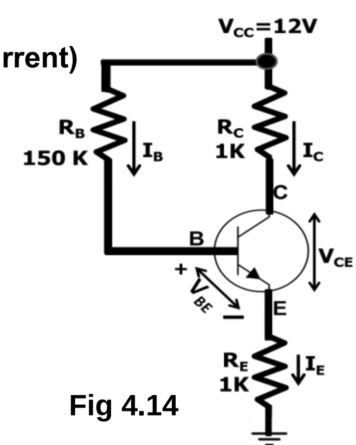


Fig 4.14

Apply KVL to base circuit

$V_{CC} - (I_B \times R_B) - V_{BE} - (I_E \times R_E) = 0$

$I_E = I_C + I_B = (\beta . I_B) + I_B = I_B (\beta+1)$ (since $I_C = \beta . I_B$)

$\therefore V_{CC} - (I_B \times R_B) - V_{BE} - (\beta+1)\, I_B . R_E = 0$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E\,(\beta+1)}$$

$$= \frac{12 - 0.3\ V}{150K + (99+1)\ 1K} = \frac{11.7\ V}{250\ K} = 47\ \mu A$$

$I_C = \beta \times I_B = 47\ \mu A \times 99 =$ **4.6 mA (Q point)**

$I_E = I_B + I_C = 47\ \mu A + 4.6\ mA = 4.65\ mA$

Apply KVL to collector circuit

$V_{CC} - (I_C \times R_C) - V_{CE} - (I_E \times R_E) = 0$

$12\ V - (4.6\ mA \times 1K) - V_{CE} - (4.65\ mA \times 1K) = 0$

$V_{CE} = 12\ V - 4.6\ V - 4.65\ V$

= **2.75 V (Q Point)**

$\therefore$ **Q point = (2.75 V, 4.6 mA)**

Load line

Point A : When $I_c = 0$, $V_{CE} = V_{CC} = 12\ V$

Point B: When $V_{CE} = 0$, $I_C = \frac{V_{CC}}{R_C + R_E} = \frac{12\ V}{2K} = 6\ mA$

4.3.2 Effect of β variations.

Problem 4.7: Calculate two Q points for the base bias circuit shown in fig 4.15, when h_{FE} = 50 and h_{FE} = 100. Assume Silicon transistor.

$V_{BE} = 0.7\ V$ (Si).

$I_B = \frac{V_{CC} - V_{BE}}{R_1} = \frac{5 - 0.7\ V}{430\ K} = 10\ \mu A$

$h_{FE} = 50$	$h_{FE} = 100$
$I_C = I_B \times h_{FE}$ $= 10\ \mu A \times 50 = 0.5\ mA$	$I_C = I_B \times h_{FE}$ $= 10\ \mu A \times 100 = 1\ mA$
$V_{CE} = V_{CC} - (I_C \times R1)$ $= 5\ V - 0.5\ mA \times 2K$ $= 4\ V$	$V_{CE} = V_{CC} - (I_C \times R1)$ $= 5\ V - (1\ mA \times 2K)$ $= 3\ V$
Q Point = (4 V, 0.5 mA)	**Q point (3 V, 1 mA)**

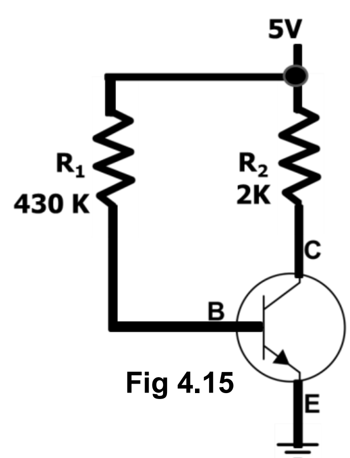


Fig 4.15

4.4 Collector to base bias (npn)

The collector to base bias circuit is shown in fig 4.16.

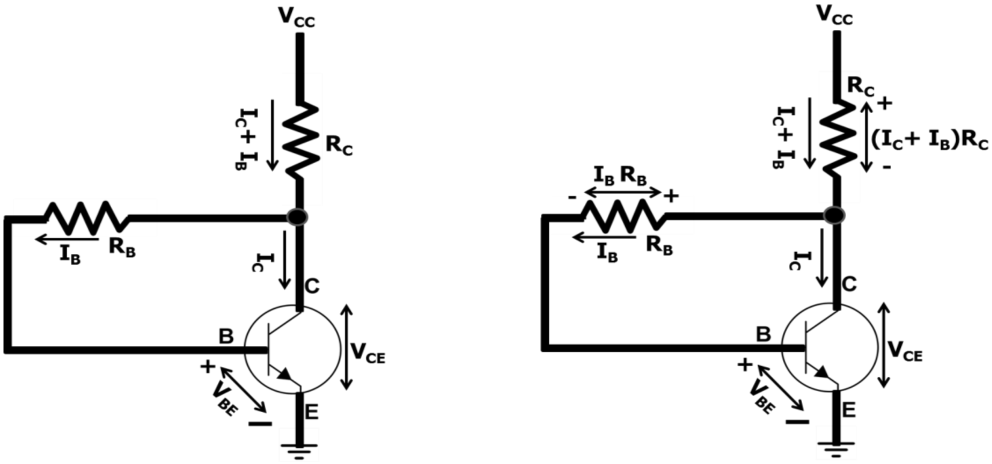


Fig 4.16

From base side

$V_{CE} = I_B R_B + V_{BE}$ 4.4.1

$I_B = \frac{V_{CC} - V_{BE}}{R_B}$ 4.4.2

From collector side

$V_{CE} = V_{CC} - (I_C + I_B) R_C$ 4.4.3

Self-stabilizing action

Collector to base works in a self-correction mode and has good bias stability.

- If I_c increases for some reason, drop across R_C increases
- Therefore V_{CE} drops.
- Because V_{CE} drops, I_B decreases.
- Because I_B decreases, I_C decreases.

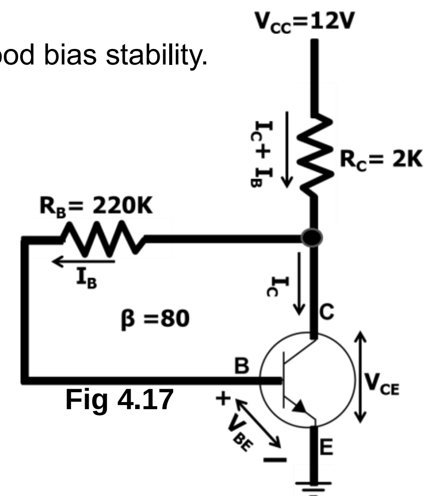


Fig 4.17

Conclusion : If I_C tends to increase, the loop prevents this Tendency

Equating both 4.4.1 and 4.4.3,

$I_B R_B + V_{BE} = V_{CC} - (I_C + I_B).R_C$

Substituting $I_C = \beta I_B$

$\therefore I_B R_B + V_{BE} = V_{CC} - [(\beta I_B + I_B).R_C]$

$I_B R_B + [I_B (\beta + 1) R_C] = V_{CC} - V_{BE}$

$$\mathbf{I_B} = \frac{V_{CC} - V_{BE}}{R_B + R_C(\beta + 1)}$$

Problem 4.8: For the germanium transistor circuit in fig 4.17, with collector-to-base bias, determine I_B, I_C, I_E, V_{CE} and Q point.

$V_{BE} = 0.3$ V (Ger)

$I_B = \frac{V_{CC} - V_{BE}}{R_B + R_C(\beta + 1)} = \frac{12 - 0.3\text{ V}}{220\text{K} + 2\text{K}(80 + 1)} = 31\ \mu\text{A}$

$I_C = \beta I_B = 80 \times 31\ \mu\text{A} = 2.48$ mA

$I_E = I_B + I_C = 31\ \mu\text{A} + 2.48\text{ mA} = 2.511$ mA **(how?)**

$V_{CE} = V_{CC} - R_C (I_C + I_B)$

$= 12\text{ V} - 2\text{K}(2.48\text{ mA} + 31\text{ mA})$

$= 7.0$ V.

Q point = (V_{CE}, I_C) = (7.0 V, 228 mA)

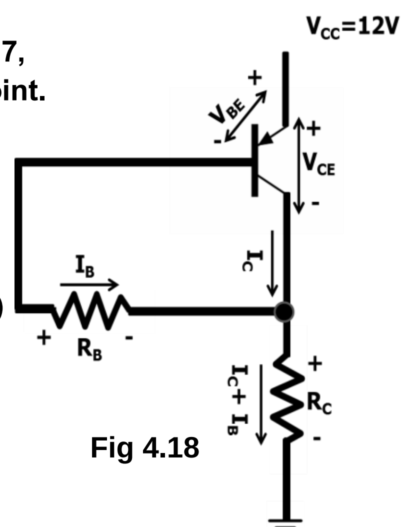


Fig 4.18

Collector to base bias (PNP) : C to B biasing of pnp is shown in fig 4.18. Reader may analyse the circuit.

4.5 Voltage divider biasing

It is the **most stable biasing technique**.

Look at the figure 4.19.

Two resistors R1 and R2 are connected in the base circuit, as potential divider. The current and voltage relationships are in the figure 4.19.

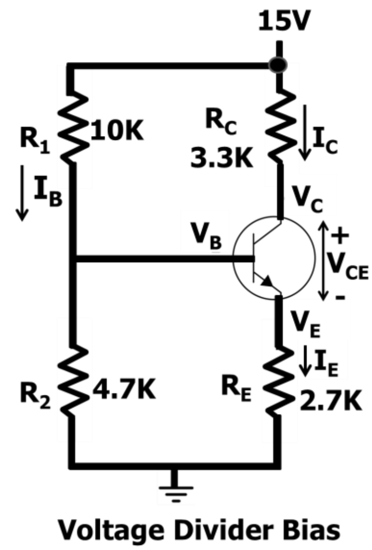


Fig 4.19

1) $\mathbf{V_B} = \frac{V_{CC} \times R2}{R_1 + R_2}$ (5 - 7.1)

2) $V_E = V_B - V_{BE}$ (5 - 7.2)

3) $I_E = \frac{V_E}{R_E} = \frac{V_B - V_{BE}}{R_E}$ (5 - 7.3)

Assume $I_E = I_C$ (neglect I_B)

5) $V_C = V_{cc} - I_C R_C$ (5 - 7.4)

4) $I_C = I_E$

6) $V_{CE} = V_C - V_E$ (5 - 7.5)

7) $V_{CE} = V_{cc} - I_C (R_C + R_E)$ (5 - 7.6)

Circuit analysis –voltage divider bias

Let us analyse the circuit with a numerical example below.

Problem 4.9: Approximate analysis

Analyze this circuit. Neglect I_B. Find V_B, V_C, V_E, I_B, I_C, I_E and V_{CE} (silicon transistor).

1) $V_B = \frac{V_{CC} \times R2}{R_1 + R_2} = \frac{15V \times 4.7K}{10K + 4.7K}$ = **4.8 V**

2) $V_E = V_B - V_{BE} = 4.8 - 0.7$ = **4.1 V**

3) $I_E = \frac{V_E}{R_E} = \frac{4.1V}{2,7K}$ = **1.5 mA**

Assume $I_E = I_C$ (Neglect I_B)

4) $\therefore I_C = 1.5$ mA

5) $V_C = V_{cc} - I_c R_c = 15$ V – (1.5 mA X 3.3 K) = **10 V**

6) $V_{CE} = V_C - V_E = 10$ V – 4.1 V = **5.9 V**

Q point = (5.9 V, 1.5 mA)

4.5.1 Thevenin Analysis → precise analysis

How to determine a Thevenin's equivalent circuit ?

Assume $h_{FE} = \beta = 50$

Problem 4.10: Analyze the same circuit precisely, (using Thevenin's equivalent)

$\mathbf{V_{Th}} = \frac{V_{CC} \times R2}{R_1 + R_2} = \frac{15V \times 4.7K}{10K + 4.7K} = 4.8$ V

$\mathbf{R_{Th}}$ = R1 ll R2 $= \frac{R1 \times R2}{R1 + R2} = \frac{10K \times 4.7K}{10K + 4.7K} = 3.2$ K

Look at the modified circuit in fig 4.20.

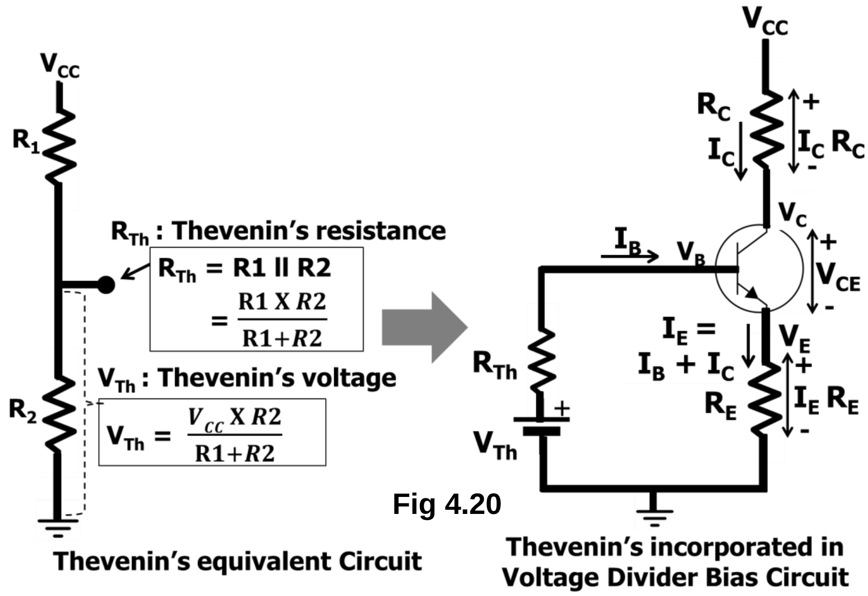


Fig 4.20

Following KVL,

$\mathbf{V_{Th} \quad = \; I_B R_{Th} + V_{BE} + R_E (I_B + I_C)}$

$I_C \quad = \; h_{FE} \times I_B = \; \beta . I_B \qquad$ (since $h_{FE} = \beta$)

$\therefore V_{Th} \quad = I_B R_{Th} + V_{BE} + R_E I_B (1 + \beta)$

$\therefore I_B \quad = \frac{V_{Th} - V_{BE}}{R_{Th} + R_E (1 + \beta)}$

$I_B \quad = \frac{V_{Th}}{R_{Th} + R_E (\beta + 1)} \qquad = \frac{4.8V - 0.7V}{3.2K + 2.7K (1 + 50)} = \mathbf{29 \ \mu A}.$

$I_C \quad = h_{FE} \times I_B$

$\quad = 50 \times 29 \ \mu A \qquad = \mathbf{1.45 \ mA}$

$I_E \quad = \; I_B + I_C$

$\quad = \; 29 \ \mu A + 1.45 \ mA \qquad = \mathbf{1.479 \ mA}$

$V_E \quad = \; I_E R_E \quad = \; 1.479 \ mA \times 2.7K \quad = \mathbf{4.0 \ V}$

$V_C \quad = \; V_{cc} - I_c R_c \quad = \; 15V - (1.45 \ mA \times 3.3 \ K) \; = \mathbf{10.215V}$

$V_{CE} \quad = \; V_C - V_E \quad = \; 10.215 \ V - 4.0 \ V. \quad = \mathbf{6.215V}$

Q point = (6.125 V , 1.45 mA)

Numerical example

Problem 4.11: Draw a DC load line for problem 4.9.

Point A: When $I_C = 0$, $V_{CE} = V_{CC} =$ **15 V.**

Point B: When $V_{CE} = 0$, $\quad I_C = \frac{V_{CC}}{R_C + R_E} \quad = \frac{15V}{3K3+2K7} = 2.5$ mA.

$\therefore$ Draw a load line with A **(15 V, 0 mA)** and B **(0 V, 2.5 mA)**

Q point from problem 4.10 = (V_{CE} , I_C) = **(6.215 V , 1.45 mA)**

Load line is drawn as shown in fig 4.21

4.6 Voltage divider, bias circuit for PNP transistor.

The voltage divider using PnP transistor is shown in fig 4.22. Compare this with npn circuit. Note, in pnp the emitter and R_E are normally drawn at the top, and the collector and R_C are drawn at the bottom. Biasing resistors R1, and R2 are inverted.

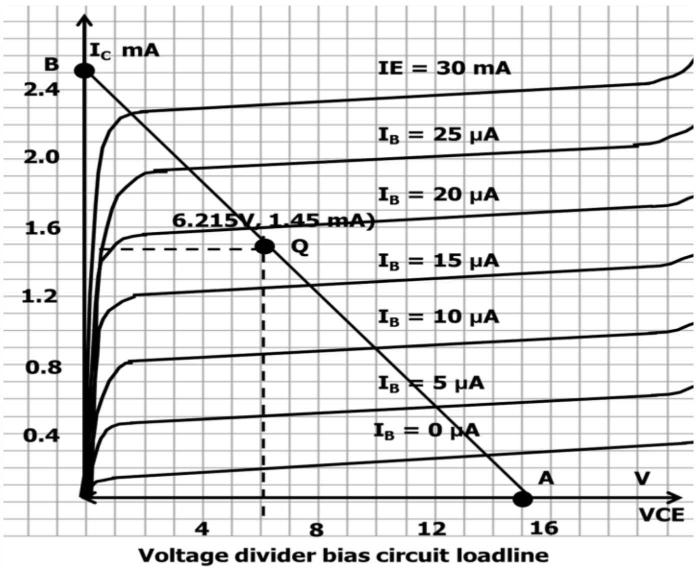


Fig 4.21

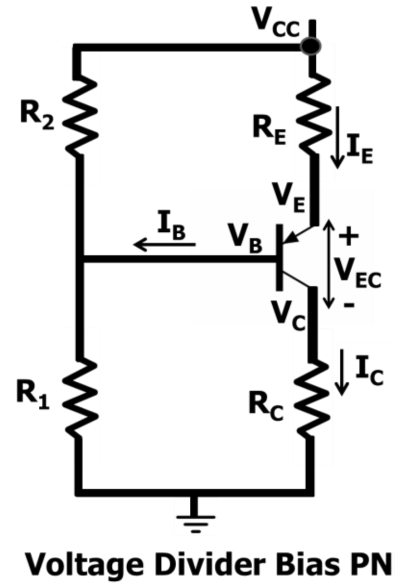


Fig 4.22

What is Alpha cut-off frequency f_α ?

Alpha cut-off frequency f_α is the frequency at which the common base DC current gain α drops to 0.707 of its low frequency value. The common base DC current gain $\alpha = \frac{I_C}{I_E}$

What is Beta cut-off frequency f_β ?

Beta cut-off frequency f_β is the frequency at which the common emitter current gain β value drops to 0.707 of its low frequency value. The common emitter DC current gain $\beta = \frac{I_C}{I_B}$

4.7 Transistor Hybrid Model (h parameters)

What is the purpose of h parameter Hybrid model?

h parameter modelling was used to predict the behaviour of a device in a particular operating region. The **small-signal ac response can be described by the hybrid model**.
This h parameter model is no longer being used

4.7.1 Two port devices & Network Parameters:-

A transistor can be treated as a two part network. The terminal behaviour of any two part network can be specified by the terminal voltages V_1 & V_2 at parts 1 & 2 respectively and current i_1 and i_2, entering parts 1 & 2, respectively, as shown in figure.

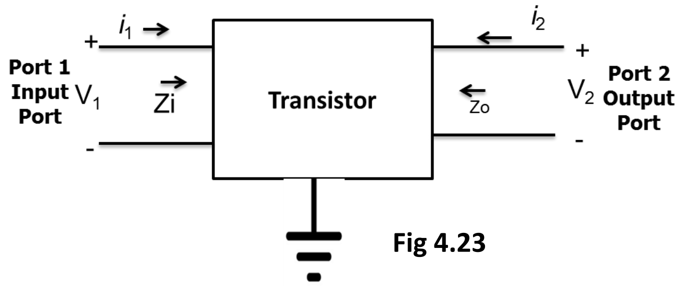


Fig 4.23

4.7.2 Two port network

Of these four variables V_1, V_2, i_1 and i_2, two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two part parameters out of which we will look at H – Parameters (or) Hybrid parameters.

<u>Hybrid parameters (or) h – parameters</u>:-
If the input current i_1 and output Voltage V_2 are takes as independent variables, the input voltage V_1 and output current i_2 can be written as

$$V_1 = h_{11}\, i_1 + h_{12}\, V_2$$
$$i_2 = h_{21}\, i_1 + h_{22}\, V_2$$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows.

$h_{11} = [V_1 / i_1]$ with $V_2 = 0$
= Input Impedance with output part short circuited (expressed in ohms)

$h_{22} = [i_2 / V_2]$ with $i_1 = 0$
= Output admittance with input part open circuited. (expressed in mhos)

$h_{12} = [V_1 / V_2]$ with $i_1 = 0$
= reverse voltage transfer ratio with input part open circuited. (No dimensions)

$h_{21} = [i_2 / i_1]$ with $V_2 = 0$
= Forward current gain with output part short circuited. (No dimensions)

Necessity of h parameter model

<u>Notations used in transistor circuits</u>:-

$h_{ie} = h_{11e}$ = Short circuit input impedance
$h_{0e} = h_{22e}$ = Open circuit output admittance
$h_{re} = h_{12e}$ = Open circuit reverse voltage transfer ratio
$h_{fe} = h_{21e}$ = Short circuit forward current Gain.

4.7.3 The Hybrid Model for Two-port Network:-

$$\mathbf{V_1 = h_{11}\, i_1 + h_{12}\, V_2}$$
$$\mathbf{I_2 = h_1\, i_1 + h_{22}\, V_2}$$

$V_1 = h_1\, i_1 + h_r\, V_2$

$I_2 = h_f\, i_1 + h_0\, V_2$

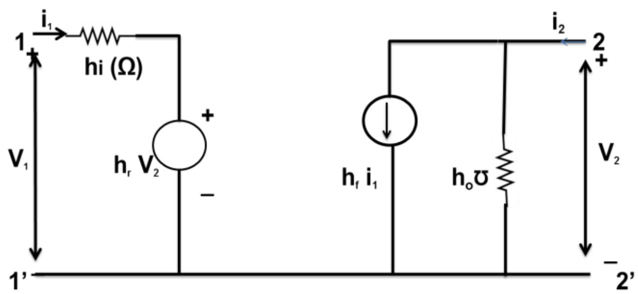
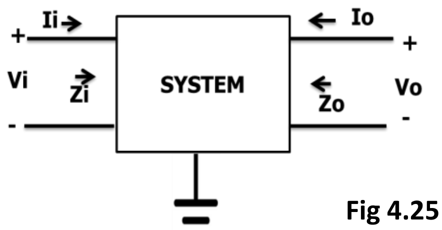


Fig 4.24 **The Hybrid Model for Two-port Network**

4.7.4 Transistor h parameters analysis of a - RC Coupled amplifier

Refer figure



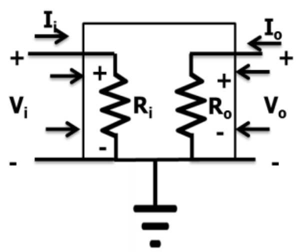


Fig 4.25

Defining the important parameters of any system.

demonstrating the reason for the defined directions and polarities.

The parameters of this Fig are

1. Input current I_i and output current I_o
2. Z_i is the impedance "looking into" the system
3. Z_o is the impedance "looking back into" the system from the output side.
4. Both the input impedance and output impedance are defined as having positive values.

$Z_i = V_i / I_i$ and $Z_o = V_o / I_o$

A RC coupled amplifier and its equivalent are shown below.

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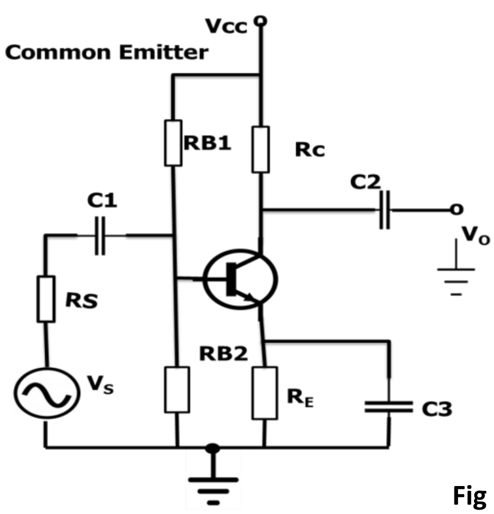


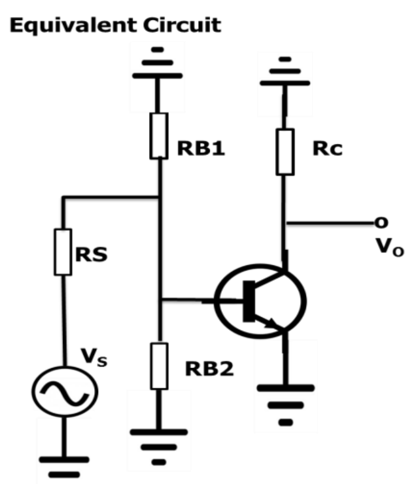


Fig 4.26

Reactance values of coupling capacitors C1 and C2 and by pass capacitor C3 will all be very low and can be replaced by shorts. The power supply points will have very low impedance for ac signals thanks to hefty filter capacitors

The equivalent circuit is on the right hand side.diagram. V_s is the input signal generator with a source impedance R_s.

From the diagram, the input impedance will be RB1 || RB2.. The resultant figure is shown below.

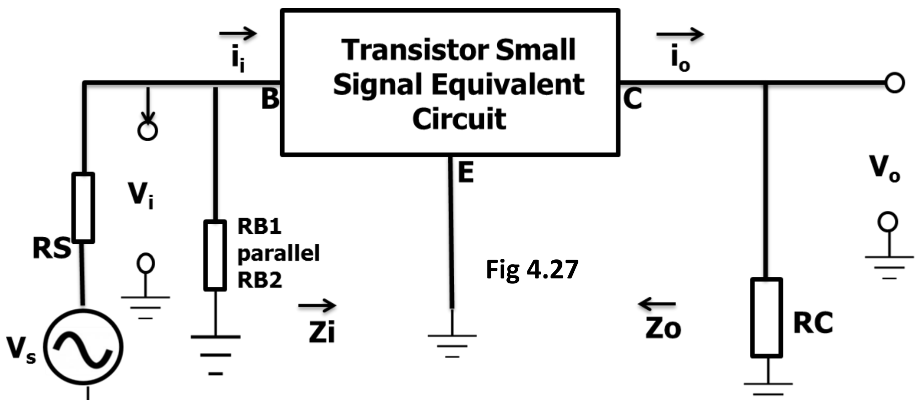


Fig 4.27

The rectangle represents the small signal ac equivalent of the transistor.

The hybrid model as we know for a common emitter configuration is

h_{ie}	input impedance (ohms)
h_{re}	reverse voltage ratio (dimensionless)
h_{fe}	forward current transfer ratio (dimensionless)
h_{oe}	output admittance (Siemen)

Note: Lower case suffixes indicate small signal values and the last suffix indicates the mode. Therefore

h_{ie} is input impedance in common emitter

h_{fb} would be forward current transfer ration in common base mode, etc.

The hybrid model for the BJT in common emitter mode is shown below:

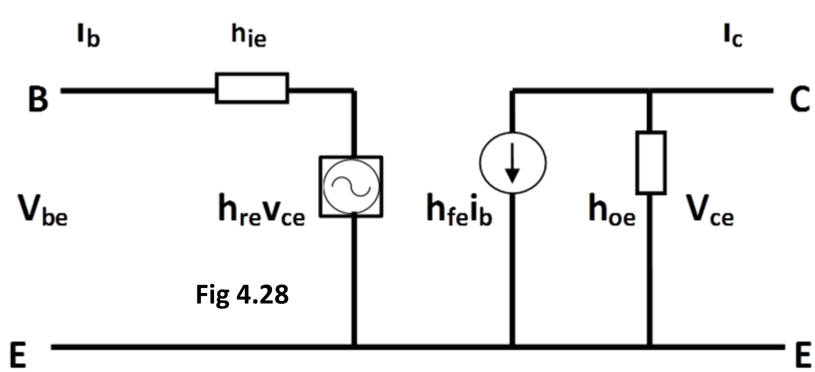


Fig 4.28

This hybrid model is accurate enough for small signals at mid band.

Two equations using h parameters can be derived from the diagram, in terms of voltage v_{be} and output i_c:

$v_{be} = h_{ie}\, i_b + h_{re}\, v_{ce}$
$i_c = h_{fe}\, i_b + h_{oe}\, v_{ce}$

If i_b is held constant (i_b=0) then h_{re} and h_{oe} can be solved:
$h_{re} = v_{be} / v_{ce} \mid i_b = 0$
$h_{oe} = i_c / v_{ce} \mid i_b = 0$

Also if v_{ce} is held constant (v_{ce}=0) then h_{ie} and h_{fe} can be solved:
$h_{ie} = v_{be} / i_b \mid v_{ce} = 0$
hfe = $i_c / i_b \mid v_{ce} = 0$

These are the four basic p parameters for a BJT in common emitter.
Typical values are

$h_{re} = 1 \text{ x}10^{-4}$,
h_{oe} = 20 mhos
h_{ie} = 1k to 20k
h_{fe} = 50 - 750.

The H-parameters can be found on the transistor datasheets.
The table below lists the four h-parameters for the BJT in common base and common collector (emitter follower) mode.

h-parameters of Bipolar Junction Transistor

Common Base	Common Emitter	Common Collector	Definitions
$h_{ib} = \frac{v_{eb}}{i_e}$	$h_{ie} = \frac{v_{be}}{i_b}$	$h_{ic} = \frac{v_{bc}}{i_b}$	Input Impedance with Output Short Circuit
$h_{rb} = \frac{v_{eb}}{v_{cb}}$	$h_{re} = \frac{v_{be}}{v_{ce}}$	$h_{rc} = \frac{v_{bc}}{v_{ec}}$	Reverse Voltage Ratio Input Open Circuit
$h_{fb} = \frac{i_c}{i_e}$	$h_{fe} = \frac{i_c}{i_b}$	$h_{fc} = \frac{i_e}{i_b}$	Forward Current Gain Output Short Circuit
$h_{ob} = \frac{i_c}{v_{cb}}$	$h_{oe} = \frac{i_c}{v_{ce}}$	$h_{oc} = \frac{i_e}{v_{ec}}$	Output Admittance Input Open Circuit

Example

Consider a Common Emitter RC coupled amplifier with RE Bypass capacitor.

We will derive expressions for voltage gain, current gain, input and output impedance. Refer figure below

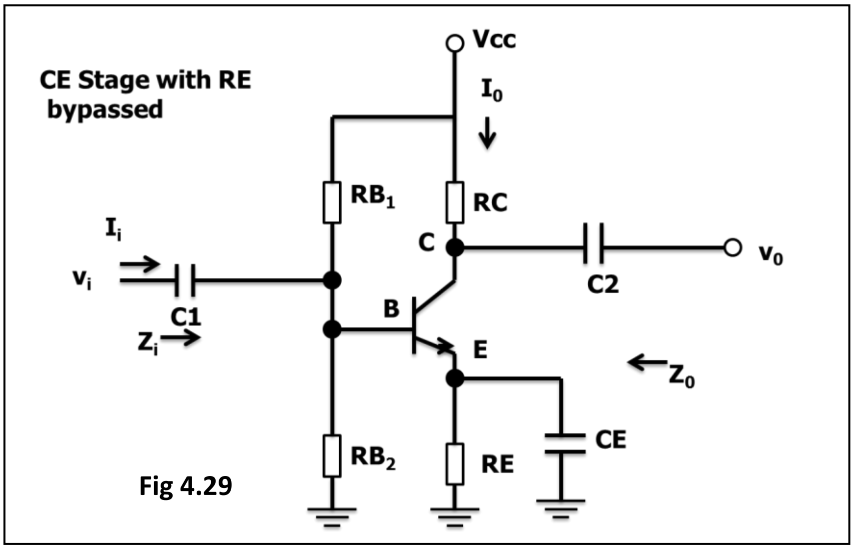


Fig 4.29

The small signal parameter $h_{re}V_{ce}$ is too small and can be neglected.

Therefore, the input resistance is just h_{ie}.

Similarly, output resistance hoe is quite large and can be neglected.

The simplified h-parameter equivalent is shown below:

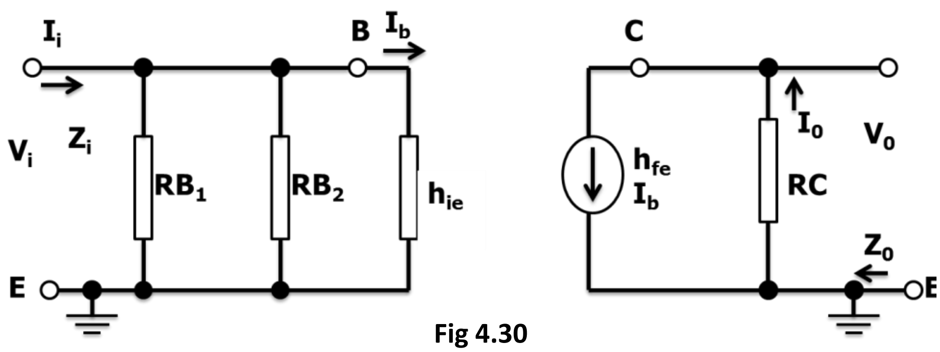


Fig 4.30

4.7.5 Input Impedance Zi

RBB will represent the parallel combination of Resistors RB1 and RB2.

R_{BB} = RB1 || RB2 =(RB1 RB2)/ (RB1 + RB2)

Also R_{BB} is in parallel with h_{ie}

Therefore input impedance $Z_i = R_{BB} \| h_{ie}$

4.7.6 Output Impedance Zo

$h_{fe}I_b$ is an ideal current generator with infinite output impedance, then output impedance looking into the circuit is:

$Z_o = R_C$

Voltage Gain Av

$V_o = -I_o\, RC$

$\quad = -\, h_{fe}\, I_b\, RC$

But $I_b = V_i / h_{ie}$ then:

Therefore $V_o = -\frac{-h_{fe}}{h_{ie}} V_i \, RC$

$Av = \frac{v_o}{v_i} = \frac{-h_{fe}}{h_{ie}} RC$

Current Gain Ai

The current gain is the ratio I_o / I_i. At the input the current is split between the parallel branch RBB and h_{ie}. So looking at the equivalent h-parameter model again (shown below):

Limitations: The hybrid model always is for a specific set of operating conditions for accuracy. If any of the device parameters vary, then the h parameters need to be recalculated..

4.8 High frequency hybrid Pi or Giacoletto model of BJT

Introduction to High frequency hybrid Pi or Giacoletto model of BJT

The **low frequency small signal model** of BJT is good enough up to 1 MHz. For frequencies greater than 1 MHz, the response of internal and parasitic capacitances needs to be taken into account. These capacitances do affect the performance of BJT at higher frequencies.

The high frequency small signal model of transistor shown below takes into account the effects of internal and parasitic capacitance's encountered in BJTs.

This **high frequency hybrid pi model** is also called as **Giacoletto model.**

What are the effects on BJT at high frequencies?

- The internal feedback capacitances reduce the gain at high frequencies.

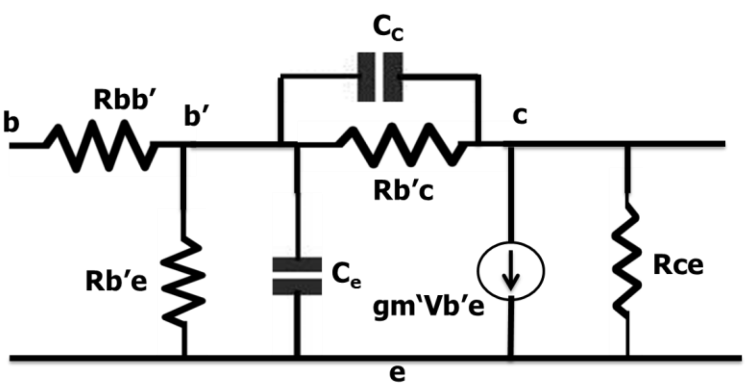


Fig 4.31

High frequency Model of BJT

- BJTs therefore will have a high frequency performance deficiency.
- The capacitances will store charges and therefore limit the switching speeds of the BJTs and therefore high speed switching circuits will underperform..

Where

g_m = Transconductance

B' = internal reference point in base

$R_{bb'}$ = Base spreading resistance

$R_{b'e}$ = Internal resistance between b' and e

$R_{b'c}$ = Feedback resistance between b' and c

R_{ce} = collector to emitter resistance

C_e = emitter base junction diffusion capacitance

C_c = transition or space charge capacitance of base collector junction.

4.8.1 Physical explanation of parameters of high frequency model of BJT

$R_{bb'}$: Base spreading resistance. It is the resistance of the semiconductor material between the external base terminal and the internal contact point inside the transistor which is inaccessible. Typically value: A few hundred ohms.

$R_{b'e}$: Internal resistance between b' and e.This represents increase in recombination base current (very less really) when emitter current increases. It shunts the collector circuit and reduces the collector current value from emitter current. Typically value: A few kilo ohms.

$R_{b'c}$: Feedback resistance from B' to C.internal base node to collector node. It simulates "early effect". **What is early effect?** If reverse bias of collector junction is increased, collector current increases as a feedback response. This feedback effect is called "early effect" and this is represented by $R_{b'c}$.

R_{ce} : This is the bulk resistance of the semiconductor material between collector to emitter.

C_e: Diffusion capacitance of emitter base junction. We know

$C_e = \tau_F * I_E / V_T$

C_C : Transition or space charge capacitance.

g_m → Trans conductance: the ratio of the change in current at the output terminal to the change in the voltage at the input terminal of an active device. In a BJT, $g_m = \frac{dI_c}{dV_{be}}$

4.9 Common emitter RC coupled amplifier.

The circuit diagram of a single stage common emitter RC coupled amplifier using transistor is shown in Fig

C_{in} : This capacitor has two major roles. It blocks any DC (both ways) between this RC amplifier and the previous stage. It also couples the ac signal from the previous stage.

The value must be fairly large (in microfarads) for low frequency response to improve.

The choice of lower values for coupling capacitors result in poor performance in lower frequencies

R1 and R2: These are the biasing resistors which sets the value of the base bias as per design requirement...

For a transistor amplifier to function properly, it should operate in the active region. Larger values of R1 and R2 increases the input impedance, a highly desirable property.

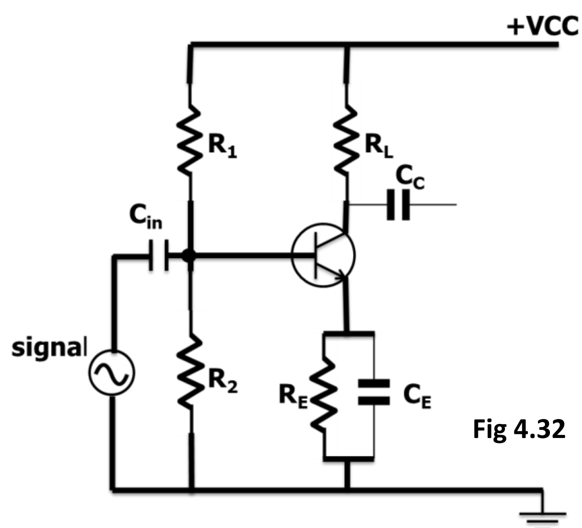


Fig 4.32

C_{out}: This capacitor also has two major roles. It blocks any DC (both ways) between this RC amplifier and the previous stage. It also couples the ac signal from the previous stage.

The value must be fairly large (in microfarads) for low frequency response to improve.
The choice of lower values for coupling capacitors result in poor performance in lower frequencies.

R_c : This is the collector resistor and R_e is the emitter resistor. The Q point (operating point) of a transistor amplifier is determined based on the amplifier requirements and accordingly R_c and R_e are selected.
Selection of R_c and R_e **in general (a thumb rule really)** will be such that 50% of V_{cc} gets dropped across the collector & emitter of the transistor and 10% of Vcc will be the emitter voltage..
This is done to ensure that the operating point is positioned at the center of the load line. 40% of Vcc is dropped across Rc and 10% of Vcc is dropped across Re.

C_e : This is the emitter by-pass capacitor. At zero signal condition (i.e, no input) only the quiescent current (set by the biasing resistors R1 and R2 flows through the R_e). C_e has no role in handling DC. When ac input signal is applied, C_e presents a low reactance across R_e and increases the gain for ac signals. Ce acts as a bypass capacitor for ac signals. The choice of lower values for C_e affects low frequency performance of the amplifier.

4.9.2 Design of an RC coupled amplifier

RC COUPLED AMPLIFIER - BJT

AIM: Design an RC coupled single stage BJT amplifier and determine its gain and frequency response, input and output impedances.

Given VCC = 12V, IC = 4mA, β = 100.

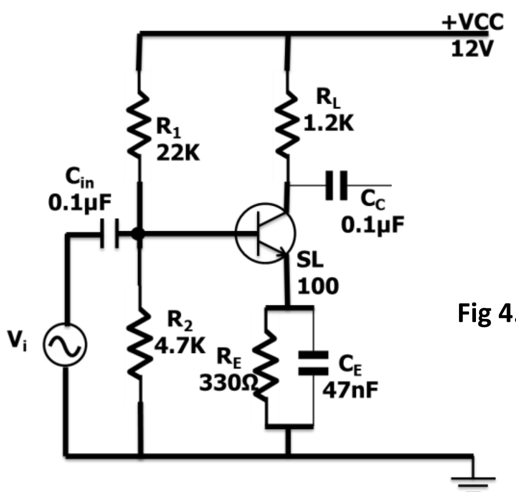


Fig 4.33

Follow these general design rules
Emitter bias (V_{RE}) = V_{cc}/10, V_{CE}= V_{cc}/2

How to find R_E:
The general design rule is (V_{RE}) = V_{cc} / 10
Therefore V_{RE} = VCC / 10 = 12 / 10 = 1.2V ------for biasing

I_E is approximately equal to I_C = 4 mA (given)

From the the circuit diagram, $I_E R_E = V_{RE}$
$R_E = 1.2 / (4 \times 10^{-3}) = 300$ ohms
Therefore Choose **R_E = 330** ohms (commercially available value)

How to find R_C:
Another general design rule is $V_{CE} = V_{CC} / 2 = 6V$ ----- for Q point to be in active region
Applying KVL to output loop
$V_{CC} – I_C R_C – V_{CE} – V_{RE} = 0$
$12 – 4 \times 10^{-3} R_C – 6 – 1.2 = 0$
Therefore **R_C = 1.2 kΩ**

How to find R_1 & R_2 ?
From biasing circuit $V_B = V_{BE} + V_{RE} = 0.7 + 1.2$
$V_B = 1.9V$
Assume 10 I_B flows through R_1 and 9 I_B flows through R_2.
We know $I_C = \beta I_B$
$4 \times 10^{-3} = 100 I_B$
Therefore $I_B = 40$ μA

$R_1 = V_{CC} – V_B / 10 I_B = 12 – 1.9 / (10 \times 40 \times 10^{-6}) = 25.25$ kΩ
Therefore Choose R_1 = 22 kΩ (commercially available value)
$R_2 = V_B / 9 I_B = 1.9 / (9 \times 40 \times 10^{-6}) = 5.28$ kΩ
Therefore Choose R2 = 4.7kΩ (commercially available value)

How to find C_E, C_C, C_B ?
Let $C_B = C_C = 0.1$ μF
Assume a very low frequency of f = 100 Hz. At this frequency, the impedance of the capacitor C_E should be 10 times lower than the resistor value R_E.
$X_{CE} = R_E/10$
Therefore X_{CE} should be = 330/10 at f = 100 Hz
$X_{CE} = 33\ \Omega$
$X_{CE} = 1 / 2\pi f C_E$
Therefore $C_E = 1 / 2\pi (100)(33) = 48$ μF Choose **C_E = 47 μF.**

4.9.3 What is the Q point of this design?

To find Q point:
V_{CE} was kept at 6V by design.
I_c was given as 4 mA.
Therefore Q point for this design is $Q(V_{CE}, I_c) = (6V, 4mA)$

Procedure to measure input impedance Zi:
1) Connect the circuit as in figure below.

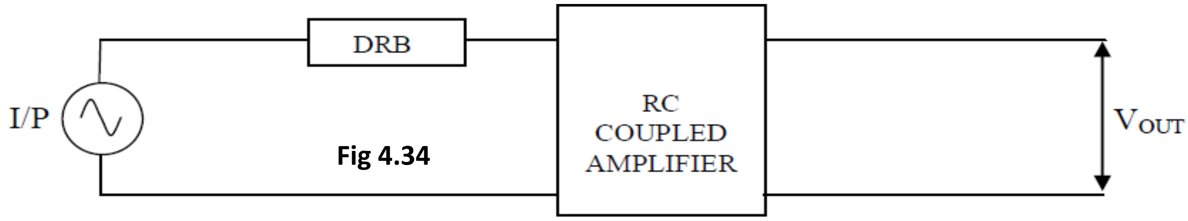


Fig 4.34

2) Set the following: DRB (Decade resistance Box) to zero. Feed a sine wave of amplitude of 40 mV at 1 KHz frequency.

3) Measure V_o(peak-peak)

4) Increase DRB till $V_O = V_o / 2$ (peak-peak). The corresponding DRB value gives the input impedance Z_i.

Procedure to measure output impedance Z_o

1) Connect the circuit as in figure below.

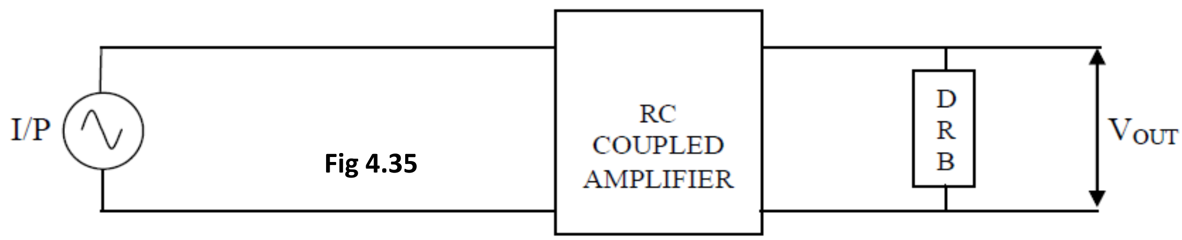


Fig 4.35

2) Set the following: DRB (Decade resistance Box) to zero. Feed a sine wave of amplitude of 40 mV at 1 KHz frequency.
3) Measure V_o(peak-peak).
4) Decrease DRB till $V_o = V_o / 2$(peak-peak). The corresponding DRB value gives the output impedance Z_o.

4.9.4 Operation of multi stage RC Coupled Amplifier

When an AC input signal is applied to the base of first transistor, it gets amplified and appears at the collector load R_L of first amplifier. This is then passed through the coupling capacitor C_C to the second stage. This becomes the input of the second stage, whose amplified output again appears across its collector load. Thus the signal is amplified in stage by stage action.

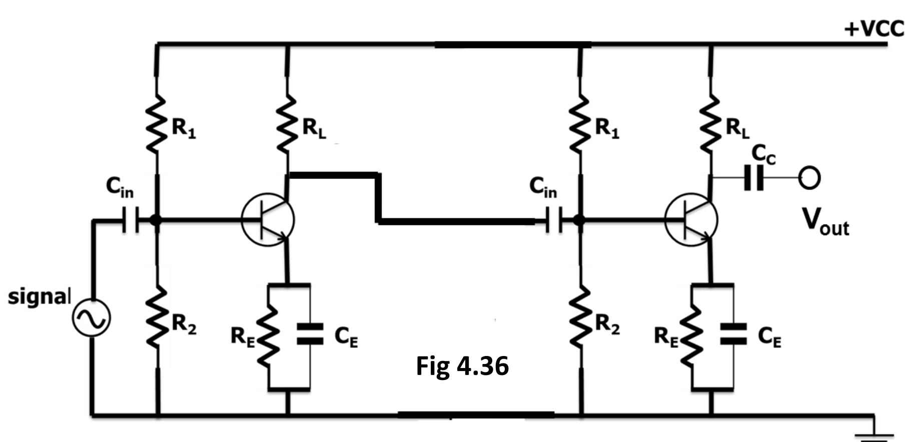


Fig 4.36

The important point that has to be noted here is that the total gain is less than the product of the gains of individual stages.

Why?

When a second stage follows the first stage, the **effective load resistance (output impedance)** of the first stage gets reduced

Why?

Due to the shunting effect of the input resistance (impedance) of the second stage.

Phase: Remember. each amplifier inverts the phase once.

Overall gain of multistage cascaded amplifiers

The overall gain of a multistage amplifier is the product of the gains of the individual stages (ignoring potential loading effects):

Gain (A) = $A_1 * A_2 * A_3 * A_4 * \ldots * A_n$.

A_1, A_2, A_3 are gains of individual stages.

4.9.5 Frequency Response of RC Coupled Amplifier

Frequency response curve is a graph that indicates the relationship between voltage gain at the output of an amplifier and as the signal frequency is varied from a very low value (say 50Hz) to a high value (say 1 MHz) The frequency response of a RC coupled amplifier is as shown in the following graph.

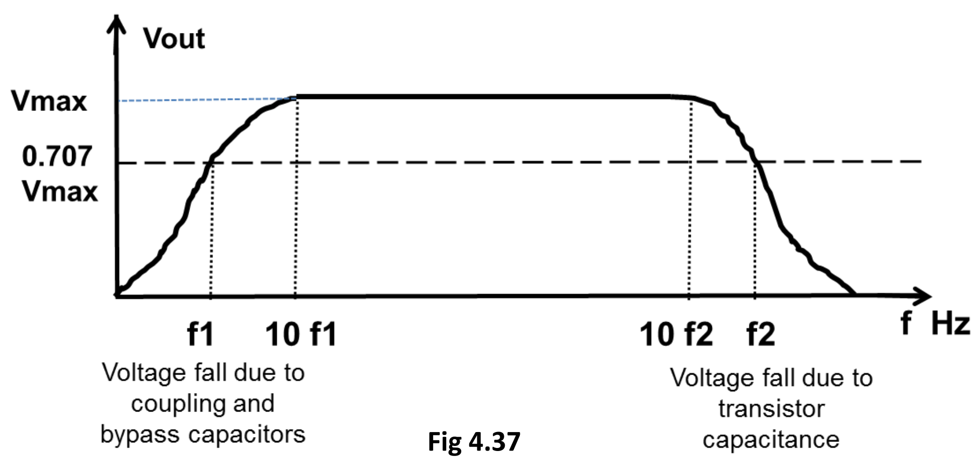


Fig 4.37

Critical frequencies:

Two critical frequencies -> f_1, f_2

These are known as - 3 dB points (corner frequencies, cutoff frequencies)

At f1 and f2 the output voltage will fall down to 0.707 times that of midband values.

Why - 3 dB?

We know dB (voltage) = 20 $\log_{10} \frac{\mathbf{V1}}{\mathbf{V2}}$. If $\frac{V1}{V2}$ = 0.707 then the dB value 0 is 20 $\log_{10}$ (0.707) = 3dB

4.9.6 What is the bandwidth of an amplifier?

The range of frequencies between f_L and f_H is called the circuits bandwidth.

Frequency points f_1 and f_2 relate to the lower corner or cut-off frequency and the upper corner or cut-off frequency points respectively were the circuits gain (or voltage level) falls off to a specific value which is 0.707 of the value at mid band.

These points on a frequency response curve are known commonly as the -3dB (decibel) points. So the bandwidth is simply given as:
Therefore **Bandwidth BW =** $\boldsymbol{f_1 - f_2}$

Mid band frequencies:
This mid band frequencies will be typically between 10 * f_1 and 0.1 * f_2.
The mid band is where an amplifier should be operated.

Example: Find the mid band of an amplifier with f_1 = 5 Hz and f_2 = 100 KHz.
10 * f_1 = 10 * 5 Hz = 50 Hz -- > lower end
0.1 * f_2 = 0.1 * 100 KHz = 10 KHz -- > upper end
Midband: 50 Hz - 10 KHz

From the above graph, it is understood that the frequency rolls off or decreases for the frequencies below 50Hz and for the frequencies above 20 KHz. whereas the voltage gain for the range of frequencies between 50Hz and 20 KHz is constant.

Figure shows the typical frequency response of an amplifier. At low frequencies the output voltage decreases because of coupling and bypass capacitors. At high frequencies, the output voltage decreases because of transistor and stray wiring capacitance

What is Alpha cut-off frequency of a transistor?
Alpha cut-off frequency f_α is the frequency at which the **common base DC current gain α** drops to 0.707 of its low frequency value. The common base DC current gain **α =** $\boldsymbol{\frac{I_C}{I_E}}$

What is Beta cut-off frequency of a transistor?
Beta cut-off frequency f_β is the frequency at which the **common emitter current gain β** value drops to 0.707 of its low frequency value. The common emitter DC current gain **β =** $\boldsymbol{\frac{I_C}{I_B}}$

Advantages of RC Coupled Amplifier
The following are the advantages of RC coupled amplifier.
- The frequency response of RC amplifier provides constant gain over a wide frequency range, hence most suitable for audio applications.
- The circuit is simple and has lower cost because it employs resistors and capacitors which are cheap.
- It becomes more compact with the upgrading technology.

Disadvantages of RC Coupled Amplifier
The following are the disadvantages of RC coupled amplifier.
- The voltage and power gain are low because of the effective load resistance.
- They become noisy with age.
- Due to poor impedance matching, power transfer will be low.

Applications of RC Coupled Amplifier
The following are the applications of RC coupled amplifier.
- They have excellent audio fidelity over a wide range of frequency.
- Widely used as Voltage amplifiers
- Due to poor impedance matching, RC coupling is rarely used in the final stages.

4.10 Gain Bandwidth product of amplifiers

In Amplifiers, the gain gets reduced (drops off) at higher as well as lower frequencies. In other words, bandwidth gets reduced. Therefore to make the amplifier useful at higher frequencies, gain is sacrificed for bandwidth. Gain Bandwidth product of a given device (say transistor) is constant. High gain would mean lower bandwidth and vice versa.

In general wide band amplifiers will have lower gain and narrow band amplifies can have high gains

The gain bandwidth product (GBW) is given by **GBW = A_NBW**

Example: A transistor RC coupled amplifier, with a gain of 10K has a bandwidth of 200 Hz. What is the GBW?
GBW = 10K X 200 Hz = 2 MHz

Overall Bandwidth of a n stage cascaded amplifier
As more number of amplifiers are cascaded,

- The overall bandwidth of the cascaded chain gets reduced, It follows the GBW concept.

Or

- Gain of the chain increases and therefore bandwidth of the chain gets reduced

BW_T - Bandwidth of the total cascaded amplifiers. **BW_S** - Bandwidth of a single amplifier

The total bandwidth of a cascaded chain of amplifiers is given by the formula
$BW_T = BW_S \sqrt{(2^{\frac{1}{n}} - 1)}$ n→ Number of amplifiers in the chain

Example: What is the total bandwidth of a 3 amplifier cascade chain if GBW = 10MHz and Gain of individual amplifier is 10
BW_S = 10 MHz/ 10 = 1 MHz
BW_T = 1 MHz ($\sqrt{(2^{\frac{1}{4}} - 1)}$ = 1 MHz X 0.435 = 0.435 MHz
Note: In this example, even though the individual amplifiers have a bandwidth of 1 MHz, the overall bandwidth of the chain comes down to 0.435 MHz.

4.11 Noise Figure:

Noise figure (NF) and N**oise Factor** (F) are measures of degradation of the signal-to-**noise** ratio (SNR), caused by components in a signal chain (say amplifier chain).
NF is just a number. This Noise Figure indicates the performance (merit) of an amplifier or a radio receiver.
Ideal Noise Figure value is 1.Lower noise figure values indicate better performance.
Noise figure is expressed in dB, always
It is the **ratio of signal to noise ratio at the output of an amplifier to the signal to noise ratio at the input of an amplifier expressed in dB.** More accurately, it can be an amplifier or a receiver or can be any electronis system really.

Noise factor (F) : It is the ratio of signal to noise ratio at the output to the signal to noise ratio at the input **expressed in number**

The noise figure is simply the noise factor expressed in <u>decibels</u>

$$F = \frac{S_i/N_i}{S_o/N_o}$$

where F= noise figure as power ratio (also known as noise factor)
Si = input signal power
Ni = input noise power
So = output signal power
No = output noise power

NF = 10 log(F)

<u>Field effect transistor (FET)</u>

4.12 Field effect transistor (FET)

- FET is a voltage operated device (BJT is a current operated device)
- FET requires (virtually) no input current but requires input voltage
- Therefore the input resistance of a FET is extremely high, a desirable property. This implies that FET circuits do not load the source or the previous stage.
- There are two major categories of FETs viz Junction FETs (JFET) and Metal Oxide Semiconductor FETs (MOSFET).
- FETs can be **n channel or p channel** devices.

N- channel JFET

- Refer figure4.38 below.
- They represent a block diagram cross section of a n channel FET.
- A n type semiconductor **(CHANNEL)** is sandwiched between two p type materials **(GATES).**
- One end of the channel is called **drain** and the other end is called the **source**.

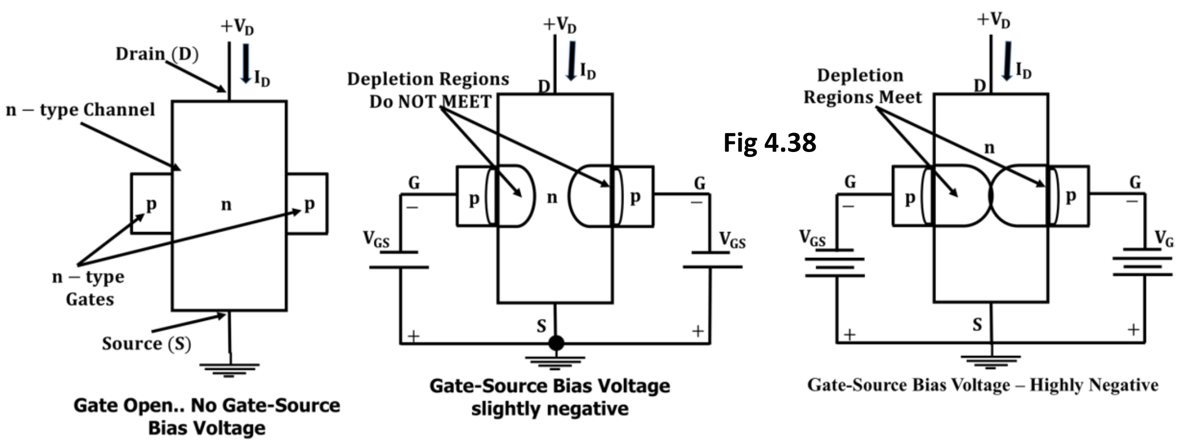


Fig 4.38

- Therefore there are three terminals to a FET viz **Source**, **Drain and a Gate**
- In a **n channel JFET, current flows from drain**, through the channel towards source. It is called the **drain current I_D**

4.13 Basic principle of operation of n Chennel JFET (nJFET):

The three figures indicate the FET action completely

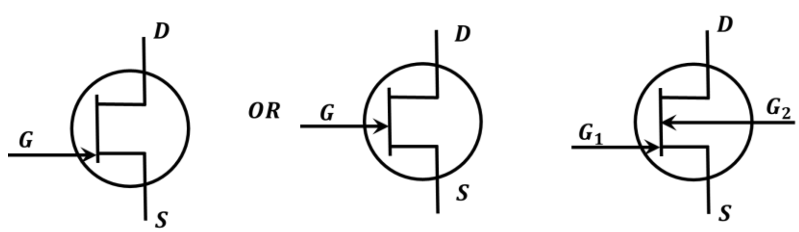
> **Fig A:** There is no voltage at the Gate. It is open. Current flows from Drain (positive) towards the Source (Negative), through the n-channel. The p type gates have no effect on the current flow.
>
> **Fig B:** The gate has a small reverse bias. From diode theory, we know, a reverse biased junction will have a depletion region which penetrates into the lightly doped region. We also know, this phenomenon is due to electric field at the reverse biased gate junction. In this case, the depletion layer penetrates into the n channel as shown in the figure. There is a **constriction** now and this **resists the current flow** through the n channel. The **drain to source current decreases** than the previous case.
>
> **Fig C:** The reverse bias is further increased. The depletion layers penetrate farther into the channel. The gates are on either side of the channel and the **depletion layers touch each other and totally block the current** in the n channel. The drain to source current becomes steady and saturated. **(pinched)**. The gate voltage at which the blockage happens, is called a **pinch off voltage.**

FET ac operation:

If an ac signal is now applied at the gate, the instantaneous voltage at the gate will go positive and negative alternately. When the bias becomes negative, the depletion layer penetration is deep and the drain current becomes less. When the bias becomes positive, the depletion layer penetration is shallow and the drain current becomes more.

The gate is normally maintained at a slight reverse bias (slightly negative voltage for nJFET so that the gate current is very low.

Why the name Field Effect Transistor?
Depletion regions are produced by the electric field at the reverse biased junction. In FETs, currents are controlled by depletion layer penetration into the channel and this happens due the effect of electric fields. Hence the name Field Effect Transistor.



N Channel JFET   Fig 4.38 a   JFET   Tetrode Connected JFET

The figure 4.38a shows the circuit symbols. The arrow for a n channel Junction FET (nJFET) is from p type gate to n type channel as shown. Both symbols are used in practice

p Channel JFET (pJFET)

A p channel JFET is shown in fig 4.39.. Note channel is p type and gates are n type. The supply voltage at Drain is negative with respect to Source. The current flow is from **Source to Drain in pJFET** (in nJFETS,the current flow is from Drain to Source).

A positive voltage at the gate of a pJFET increases reverse bias, increases depletion penetration and reduces drain current.

A negative voltage at the gate of a pJFET decreases reverse bias, decreases depletion penetration and increases drain current.

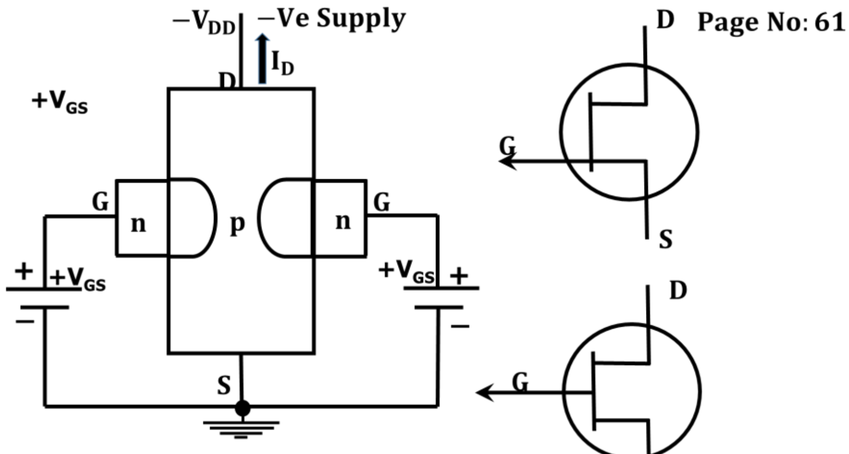


Fig 4.39

P Channel JFET

4.14 How depletion region behaves in a FET?

In a nFET we know current flows from drain to source. If we take three points A, B and C in the channel, the voltage at A will be high compared to B and C. Voltage at C will be lowest .

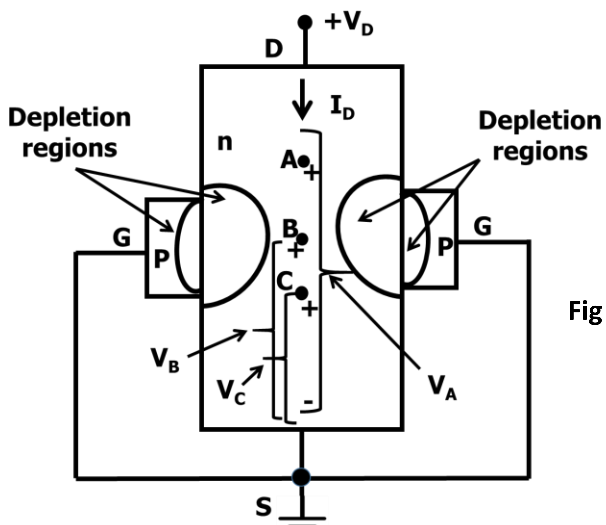


Fig 4.40

Therefore the reverse bias between Gate and A will be high, between Gate and B will be medium and between Gate and C will be least. Therefore the depletion region penetration will be maximum at A and minimum at C.

The figure 4.40 shows this skewed depletion region.

Drain Characteristics

Like the output characteristics of BJT, we can plot output characteristics (Drain Characteristics) of JFET also. Refer fig 4.41

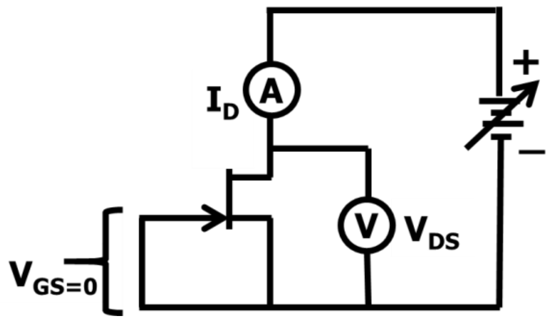


Fig 4.41

Let us keep $V_{GS} = 0$

As V_{DS} is an increased nJFET exhibits

Three distinct regions (Figure 4.42)

a) **Ohmic region**: As V_{DS} is increased gradually from OV, the current increases linearly. This implies that FET acts like a resistor. As V_{DS} increases, the depletion region approaches pinch off and FET deviates sharply from its ohmic behaviour.

b) **Pinch off region**: When V_{DS} approaches 4.5V (in our example) (Point A in figure 4.41) has a reverse bias equal to pinch off voltage. The depletion layers from both Gates touch each other beyond this. An an equilibrium (saturation) is reached and I_D does not increase even if V_{DS} is increased. This saturation current is

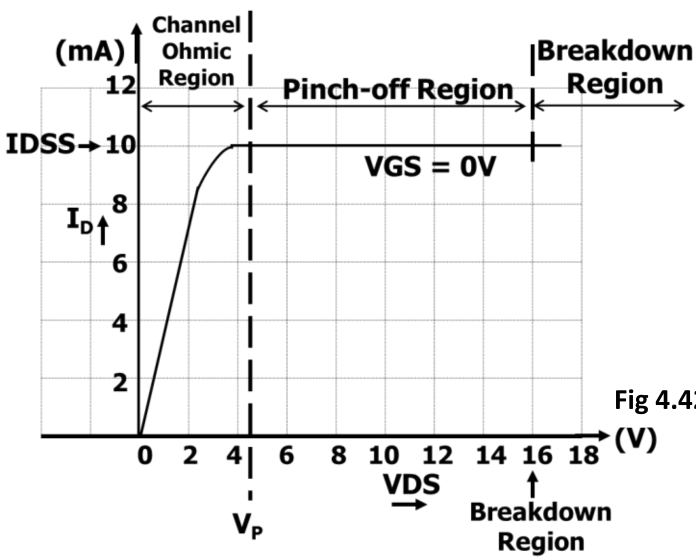


Fig 4.42

I_D Vs V_{DS} characteristics for an n-channel JFET (V_{GS}=0)

known as I_{DSS}. The drain-source voltage, where the saturation begins is pinch-off voltage (4.5V, in this example).

c) **Break down region**: If the V_{DS} increased further, at a particular voltage, the reverse biased gate-channel junction breaks down. When this happens I_D rises without control and the device may get destroyed.

What is the difference between pinch-off voltage and $V_{GS(off)}$?

Pinch off voltage (V_p): Pinch off voltage is the drain to source **voltage** after which the drain to source current becomes almost constant and **JFET** enters into saturation region and is defined only when gate to source **voltage** is zero.

$V_{GS(off)}$ voltage: It is the Cut-off Voltage of a FET. This is the voltage necessary to turn the FET off. JFETs and MOSFETs are normally on with a drain current between drain and source. However, a specific voltage **$V_{GS(off)}$** should be applied to the gate-source region to will turn the FET off, so that no current flows from drain to source.

4.15 Drain Characteristics with Bias (Fig 4.43)

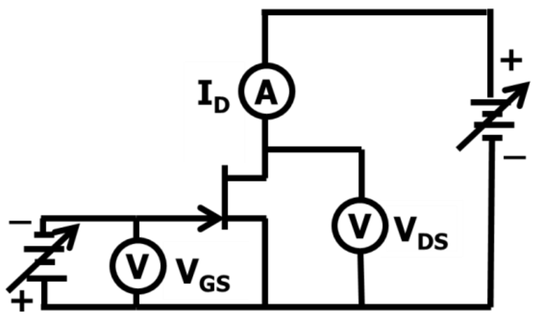


Fig 4.43

- Keep V_{GS} at -1V. Increase V_{DS} gradually from 0V to 14V and measure I_D and plot the curve.
- Repeat the same exercise for different V_{GS} values and plot a family of curves.
- As V_{GS} = -1V, there is already a fixed reverse bias of 1V. Therefore the pinch-off will occurs 1V earlier at 3.5V (when V_{GS} = 0, pinch-off = 4.5V). At V_{GS} = -2V, there is already a fixed reverse bias of 2V. Therefore the pinch-off will occurs 2V earlier at 2.5V

.

Transfer Characteristics

For an nJFET, transfer characteristics is plot of **I_D versus V_{GS}**. Refer fig.4.44. We know gate-source voltage controls I_D.

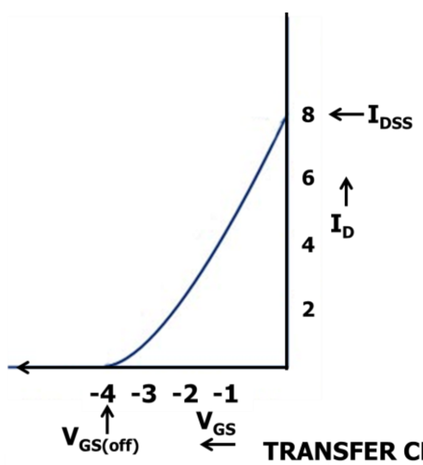
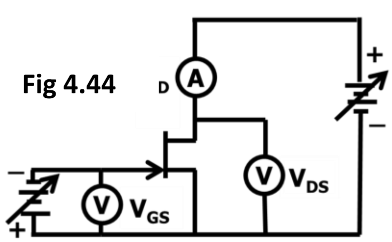


Fig 4.44



TRANSFER CHARACTERISTICS

A circuit for plotting the characteristics is shown. The characteristics extend from $I_D = I_{DSS}$ at $V_{GS} = 0$ to $I_D = 0$ at $V_{GS} = -V_{GS}$ (off).

How to choose a FET?
Begin by choosing an appropriate type number (n channel or p channel) understand the maximum rating on V_{GS} (Drain to Source voltage), Gate Current, (I_G) drain-gate voltage (V_{DG}) and reverse Gate-Source voltage ($V_{GS(r)}$), make sure your operating condition never exceed these.

How do you relate these parameters?
Example: For an nJFET 2N5457, maximum V_{DS}=25V. We need to operate the gate at V_{GS} =-3V.
What can be maximum V_{DS} permissible?
$V_{DS} = V_{DG}(max) - V_{GS} = 25-3 = 22V$

How do we find maximum drain current (I_D(max))?
Find the maximum power dissipation from the data sheet and divide it by maximum V_{DS} permissible.

Why do we have gate current I_G specified?
In a reverse bias situation of the gate, there will be negligible gate current (I_G) flow. However in situations where gate is forward biased, I_G will flow and it should be ensured that I_G is kept below the maximum value specified.

What is the saturation current in a FET?
We learnt that the drain source saturation current (I_{DSS}) is the maximum current that flows through a FET when V_{GS} =0V
(Refer fig 4.42). I_{DSS} is listed in the data sheet. In practice I_{DSS} is specified for V_{GS} value. For example, for the FET IN5457 V_{GS} can vary between -0.5V and -6V and the corresponding I_{DSS} varies between 1mA and 5mA.

The FET equation for I_D in terms of I_{DSS} is

$$\mathbf{I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2}$$

$V_{GS(off)}$ is the cut-off voltage

Example; Find the drain current I_D when $V_{GS} = 0.5V_{GS(off)}$ and I_{DSS} = 8mA

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

= 8mA $(1 - 0.5)^2$
= 8mA $(0.5)^2$
= 2mA

4.16 Forward transfer admittance (Transconductance)

It is denoted by γ_{fs}
Transconductance is an important and popular specification.

$\gamma_{fs} = \frac{\text{Variation in } I_D}{\text{Variation in } V_{GS}}$ (when V_{DS} is constant)

γ_{fs} units will be in micro siemens (μS) or micro mhos
microamps/volt ($\mu A/V$) or millisiemens (mS) or
millimhos or milliamps/volt(mA/V)

If γ_{fs} = 5mA/V, it means that the drain current (I_D) varies by 5mA when input V_{GS} changes by 1 volt

We know $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$$\gamma_{fs} = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{2I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

Example : Given $V_{GS(off)}$ = - 8V and I_{DSS} = 10 mA. Find out transconductance at V_{GS} = -2V and V_{GS} = -5V for a JFET.

$$\gamma_{fs} = \frac{2I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) = \frac{2\times10}{8}\left(1 - \frac{(-5V)}{(-8V)}\right)$$

$$= 2.5 \times \frac{3}{8} = 0.925\ \mu S$$

Output admittance (γ_{os})

$$\gamma_{os} = \frac{\Delta I_D}{\Delta V_{DS}}|V_{GS} = \frac{\text{Variation in } I_D}{\text{Variation in } V_{DS}}$$ when V_{GS} is constant

4.17 FET amplifier

A JFET amplifier is shown in fig 4.45

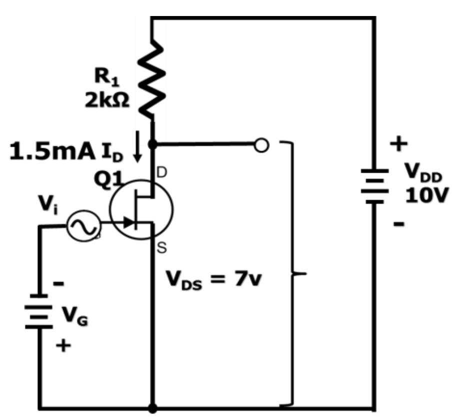


Fig 4.45

Drain is connected to the +ve supply and source is grounded (-ve terminal of the supply).
Gate source is reverse biased by a -ve power supply. An ac voltage source is connected in series.
We know FET is a voltage driven device.
As seen earlier, a change in gate source voltage (ΔV_{GS}) causes a change in drain current.
As the drain current changes, the drop across R_1 changes correspondingly.
Let V_{DD} = 10V, R = 2kΩ
Let V_{GS} be biased such that I_D = 1.5mA
Let γ_{fs} = 5000μS. The signal varies by $\pm 40mV$
The voltage at drain terminal $V_D = V_{DD} - I_D R_1$

$= 10V - 1.5mA \times 2k$

$= 7V$

The variation in drain current at +40mV :$\Delta I_D = \gamma_{fs} \times V_i$

=5000μs X 40mv
=0.2mA

Voltage V_D at drain = V_{DD} - R1(ID +ΔI_D)
= 10v-2K(1.5mA+0.2mA)
= 10v-3.4v
= 6.6v

ΔV_D = 7.0v-6.6v = 0.4v

Variation in drain current at -40mv :ΔI_D=-0.2mA

Voltage V_D at drain = V_{DD} - R1(ID −ΔI_D)
= 10v-2K(1.5mA-0.2mA)
= 10v-2.6v
= 7.4v

ΔV_D = 7.0v-7.4v = -0.4v

Output variation V_0 = ±0.4v

Input variation = ±40mv

Gain of the amplifier = A_V = $\frac{Vo}{Vi}$ = $\frac{0.4v}{40mv}$ =10

4.18 FET Switch

An FET switch is shown in figure 4,46. It looks similar to a BJT switch.

When the input voltage is zero, FET is on drain current flows. The drain voltage V_{DS} will be at ground potential. FET in this conduction state has a drain-source on resistance [$r_{DS(on)}$]. This is very much lower than the saturation resistance of BJT.

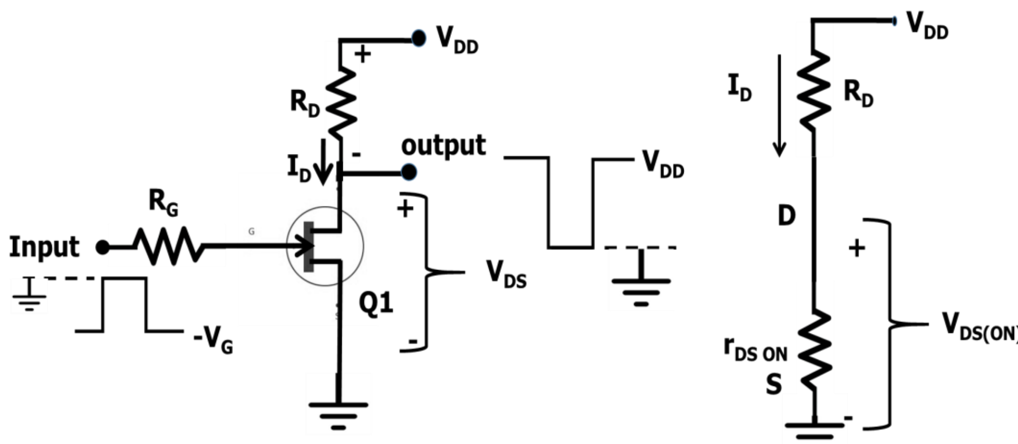


Fig 4.46

When input goes negative, FET is sufficiently reverse biased so that FET is off and no drain current flows.V_{DS}=V_{DD} in this state.

You can see when input is ZERO, output is ONE and when input is ONE, output is ZERO. It is an inverter and a switch.

BJT and FETs have switch on time and off time. These constitute, rise time, fall time and storage time, popularly termed as propagation delay. Longer the propagation delay, slower is the device.

Which is faster? BJT or FET?

FETs are faster switching devices than BJT since they do not have forward biased junctions and therefore do not have diffusion capacitance.

4.19 MOSFETS

What is a MOSFET?
Metal oxide semiconductor FET (MOSFET)
Where it is used?
Widely used in amplifiers and switching circuits

What are the differences between MOSFET and BJT?

BJT	MOSFET
3 terminal devices	3 or 4 terminal devices
Emitter, base, Collector	Source, drain, gate, body
Current controlled devices	Voltage controlled devices

4.20 Enhancement MOSFET

MOSFET is also is known as **insulated gate FET**. It consists of a p type substrate which is highly resistive on which 2 blocks of n type substrate are diffused. Refer Fig 4.47. These n type substrates are highly doped.

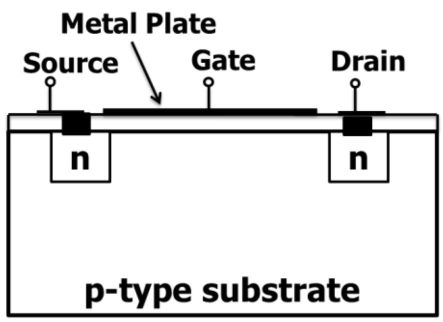
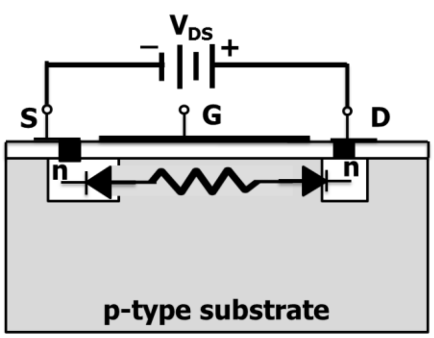


Fig 4.47

The surface is a layer of Silicon-di-oxide. Now holes are cut through the SiO_2 layer to access the n-type material. Metal is deposited through the holes, on both n-type material and designated as drain and source.

A metal deposited on the surface area between drain and source and is designated as Gate.



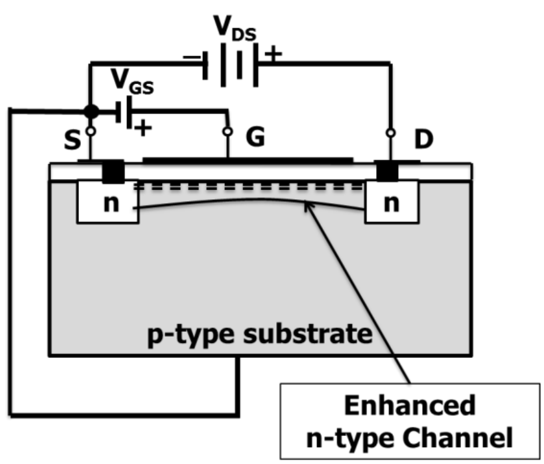


Fig 4.48

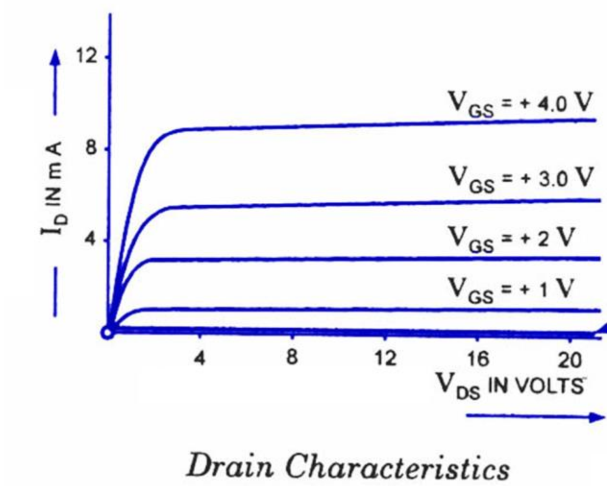
- ❑ Drain of a MOSFET is positive.
- ❑ The two n-blocks and the p block form two p-n junctions, back to back.
- ❑ The drain junction is reverse biased. Negligible current flows through it.
- ❑ In fig 4,48, source is connected to substrate.

- ❑ Apply a +ve gate voltage now.
- ❑ The negative (Minority) charge carriers (electrons in this case), are attracted towards the positive plate which is the gate.
- ❑ These electrons cannot cross SiO_2 layer hence accumulate close to the surface of the substrate as shown in figure 4.48b.
- ❑ You can now see a n channel between drain and source.
- ❑ If a gate-source voltage is made more positive, this channel accumulates more electrons. The channel resistance reduces and current starts flowing between drain and source.
- ❑ In other words, drain-source current I_D proportional to $V_{GS.}$
- ❑ The conductivity of the channel is ENHANCED by the positive gate voltage.
- ❑ So, this device is known as **enhancement MOSFET or EMOS transistor.**

MOSFET-Drain and Transfer Characteristics

Refer fig 4.49. The drain characteristics for n channel EMOS is shown.

- o As positive V_{GS} increases I_D increases
- o **There is no gate source leakage current in MOSFET-why?**
- o **By construction, Gate is insulated from the channel, thanks to SiO_2 layer. Therefore MOSFETs have an extremely high input**



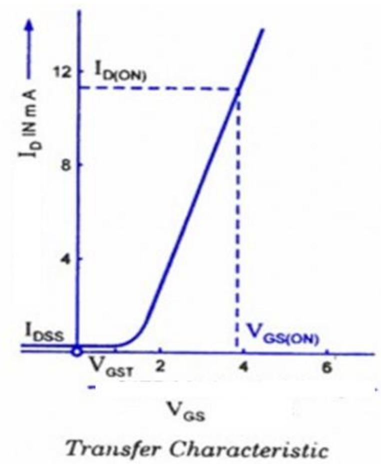


Fig 4.49

resistance (10^{15} ohms really !).

- o Like JFET, MOSFETs a transfer admittance (trans-conductance) ranging from 1ms(1mA/v) to 6ms(6mA/v)

Fig shows the graphic symbols of an n channel MOSFET, one with source and substrate connected together and another one separated.

Note: Device channel is broken into 3 sections. Why?

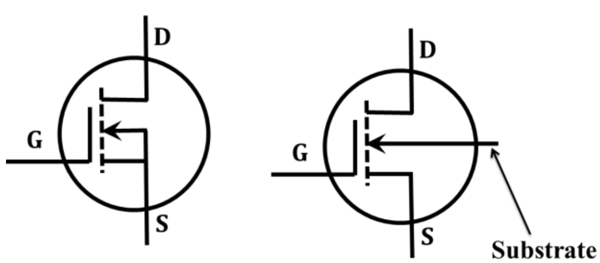


Fig 4.50

A channel does not exist until and unless a gate voltage is applied.

Note: The gate does not make contact with the channel. Why? Because gate and channel are insulated by SiO_2 layer.

P channel MOSFET

Construction is similar to N-MOSFET. Refer Fig 4.51

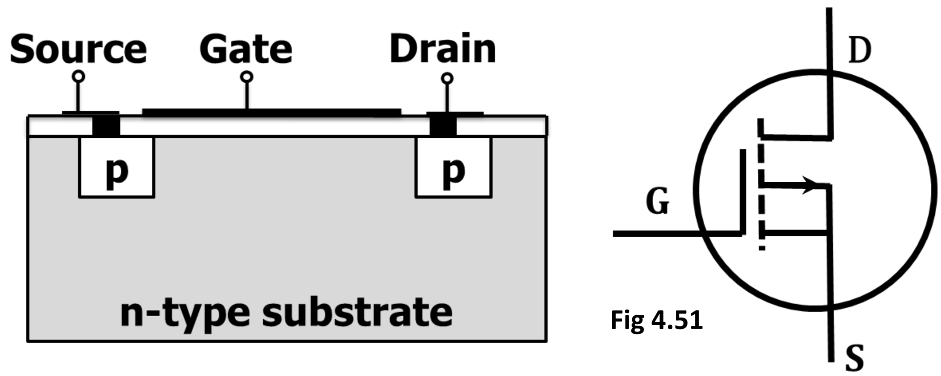


Fig 4.51

Description also is similar except that all voltages and polarities and current flows are to be reversed.

Drain to source voltage is negative

Gate –source voltage is negative.

4.21 D MOSFET –Depletion-Enhancement MOSFET (Fig 4.52).

It is similar to n channel EMOS seen already . The n type channel is lightly doped in this device. When a +VE V_{DS} is applied, a drain current I_D flows even if $V_{GS} = 0$

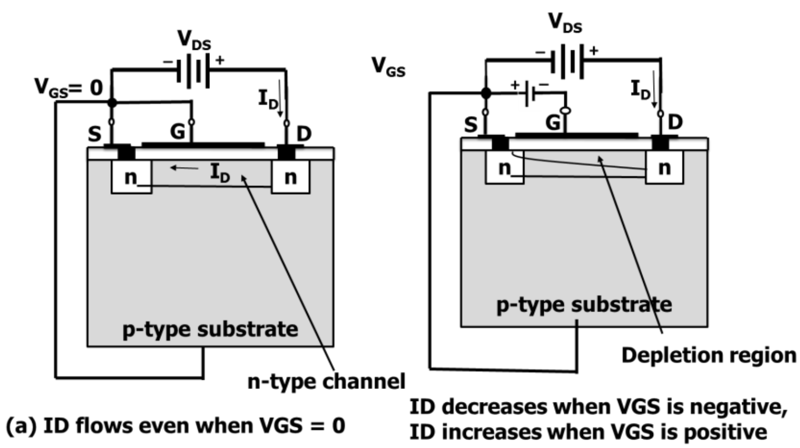


Fig 4.52 n-channel depletion-enhancement MOSFET

Some of the negative charge carriers are repelled away from the gate and move away from the "n to n" region, as shown in the figure. This creates a depletion region in the channel (n to n region) and I_D decreases. This phenomenon is similar to what happens in JFET. Hence this can be called depletion mode JFET.

Now apply a +ve V_{GS} . N type charge carriers do get attracted from the p substrate and accumulate in the channel (n to n region).This enhances conductivity and increases I_D . **Therefore depletion mode FET can also multiplex as enhancement FET. Hence this device is called depletion enhancement MOSFET or DEMOSFET or DMOSFET.**

Comparison of n and p channel FETs
n Channel FETs have lower resistivity and hence lower R_D resistance. For a given R_D, p Channel FETs are more expensive.

MOSFET Handling

They are low current devices and can be easily destroyed by Electro-Static Discharge (ESD). A person walking across a carpet can generate 20000 Volts as a static electricity, believe it or not! If that person handles a MOSFET, there may be an electrostatic discharge of such voltages from the person to the device which can potentially damage a MOSFET.
Hence, ESD (anti-static) precautions are needed while handling MOSFET devices.

1. MOSFETs should be stored in conductive containers which do not allow charge accumulation.
2. Wear anti-static globes or grounded-wrist-bands while handling MOSFET.
3. Tools such as soldering irons must have grounded tips.
4. Operator chairs must be grounded.
5. Working area should have grounded conductive carpets or conductive flooring.

4.22 VMOS FET

What is VMOS FET?
V shaped MOSFET.

Construction

VMOSFET creates vertical channels where as MOSFETS create horizontal channels. Vertical

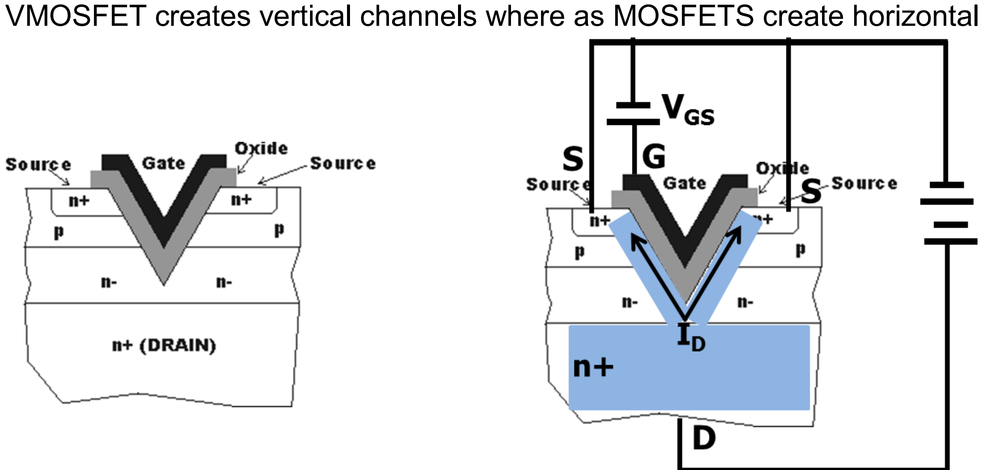


Fig 4.53

channels allow construction of small channel length, lower resistance devices with higher power handling capacities, better frequency response and high values of trans-conductance.

Refer Fig 4.53

- There is a V-CUT which expands from n+, p, n- layers, all the way up to n+ substrate.
- SiO_2 layer covers the horizontal layers and vertical grooves.
- Gate is a metallic thin plate deposited on SiO_2 layer, in the V groove.
- Drain is the bottom most n^+ substrate.
- Source is the top n^+ region and p^+ region.

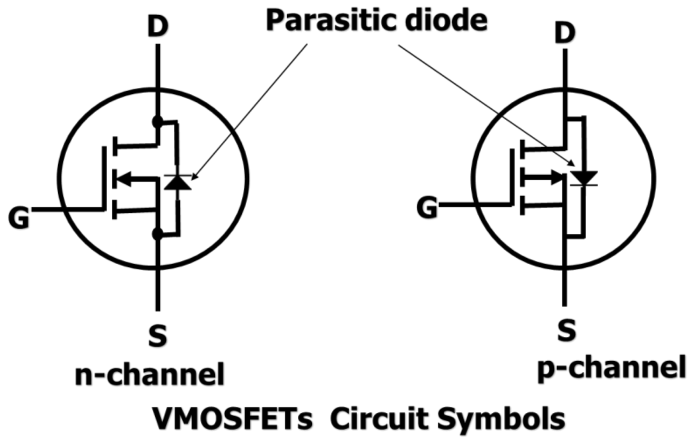


Fig 4.54

Operation

V MOSFET works on enhancement mode. In the absence of positive V_{GS}, no I_D current flows.

When V_{GS} is positive, negative charge carriers (electrons) get attracted to the positive plate which is the gate.

These electrons cannot cross the SiO_2 layer and hence accumulate, along the V groove, as shown in Figure.

Current flows vertically, from drain to source and hence the name VMOSFET.

4.23 FET Biasing

Like BJTs, FETs have biasing technologies. FETs also can be analysed using DC load lines and Q-points.

How to draw a load line for the circuit shown in Fig 4.55?

DC load lines are drawn on output characteristics (like BJT) or drain characteristics. In the figure 4.55, gate is biased to a voltage $-V_G$ through a resistor R_G**.** DC load lines will be drawn on graph of I_D and V_{DS}. In Fig 4.56

From the circuit we known $V_{DS} = V_{DD} – I_D R_1$

Case.1

When $I_D = 0$, $V_{DS} = V_{DD} – I_DR_1$

$= 22V – 0 = 22V$

Point A coordinates on Fig. 4.56

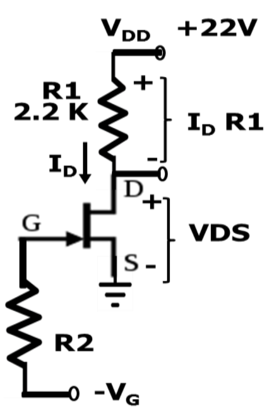


Fig 4.55

$I_D = 0$, V_{DD} = 22mA

Case 2

When $V_{DS} = 0$, $0 = V_{DD} – I_DR_1$

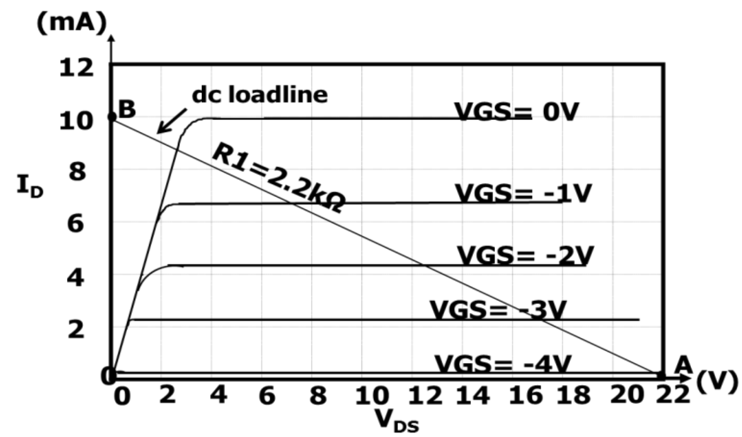
$= 22V – 2.2k\ I_D$

$I_D = 10mA$

Point B Coordinates are

$I_D = 10mA$, $V_{DD} = 0$

The DC load line AB is shown in Fig. 4.56, for $R_1 = 2.2K\Omega$.



DC load line on FET drain characteristics. Fig 4.56

Q-Point:

What is a Q-point?

It is the operating point of a FET when there is no ac signal. The coordinates are I_D and V_{DS}.
When an AC signal is applied, V_{DS} varies and therefore I_{DS} also varies.
Refer Fig. 4.57. In FET, V_{DS} must always remain in pinch off region. V_{DS} should never be allowed to fall below the Gate-Source cutoff voltage $V_{GS(off)}$, to avoid going into the ohmic region. Therefore, as a precaution, V_{DS} should always be 1V more than $V_{GS(off)}$.. A safe design should ensure a cushion.

$$\mathbf{V_{DS(min)} = V_{GS(off)} + 1V}$$

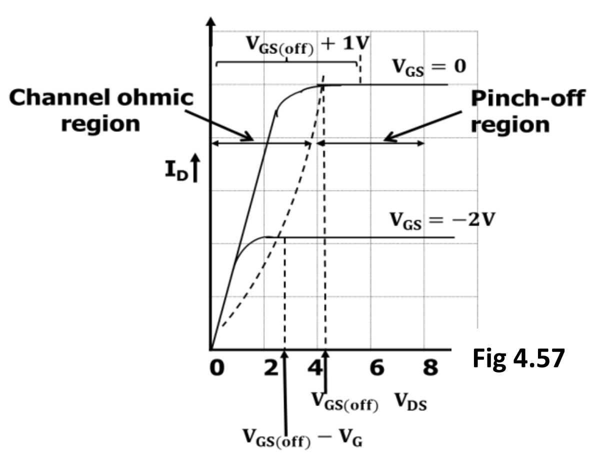


Fig 4.57

In a FET, V_{DS} must be a minimum of $V_{GS(off)} + 1V$

Also, from the figure note the actual cut-off voltage keeps shifting depending on the gate bias voltage. In the figure

When $V_{GS} = 0$ $V_{GS(Off)} = 4.5V$ $V_{DS(min)} = 5.5V$

V_{GS} = -2V $\quad$ $V_{GS(Off)}$ = 2.5V

Therefore $\quad$ $V_{DS(min)}$= $\quad$ $V_{GS(Off)} - V_{GS} + 1$

Example: For the circuit shown in Fig. 4.58, find the maximum permissible output voltage swing for Q points at V_{DS} = 10V and at V_{DS} = 16V.

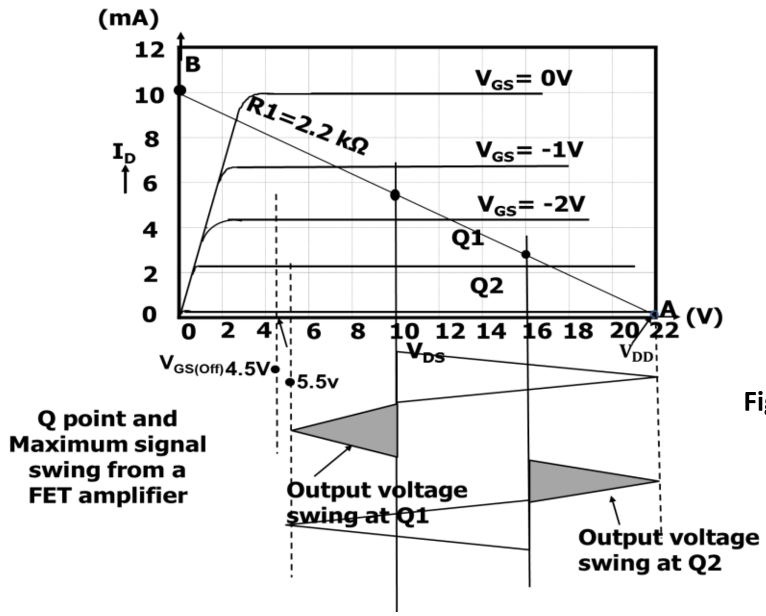


Fig 4.58

Case.1: Ass

For a Q-point at V_{DS} = 10V,

ΔV_S in the upper side = 22V – 10V = 12V

ΔV_S in the lower side = 10V – 5.5V = 4.5V

The positive swing possible is 12V.

Whereas the negative swing possible is 5.5V.

The maximum undistorted swing possible is ±5.5V.

Case.2:

For a Q-Point at V_{DS} = 16V.

The upper swing possible = 22V – 16V = 6

The lower swing possible = 16V – 4.5V = 11.5V

The maximum undistorted swing possible is ±6V only.

Source Resistance

Figures 4.59 shows resisters in the source and source+drain respectively.

$\mathbf{V_{DS} = V_{DD} - I_D R_1}$

$\mathbf{V_{DS} = V_{DD} - I_D (R_1 + R_2)}$

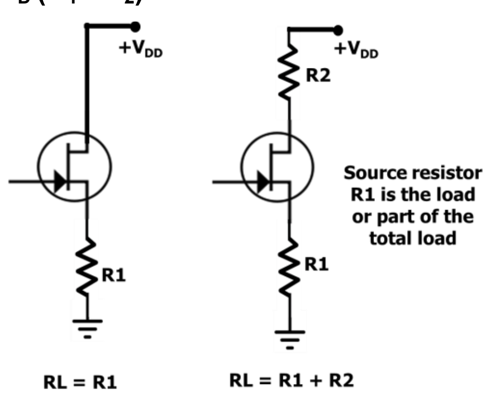


Fig 4.59

4.24 Gate Bias

FETs can be configured to operate with a gate bias as shown in Fig. 4.60. Gate is returned to a bias of -2.0V through a resistor R_2. The drain resistance R_1 (4K) is connected to a +20V supply.

Example.3:

For the circuit in Fig. 4.60, what are the $I_{D(max)}$, $I_{D(min)}$, $V_{DS(max)}$ and $V_{DS(min)}$? V_{GS} = -2V
Draw a vertical line at V_G = -2V, on the transfer function characteristics in Fig. 4.60. It intercepts, the $I_{D(max)}$ curve at 4.0 mA and $I_{D(min)}$ curve at 0.5mA.

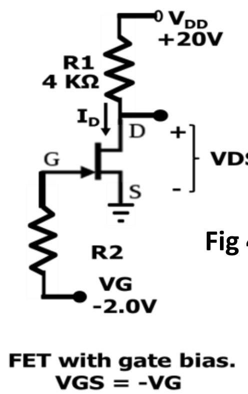


Fig 4.60

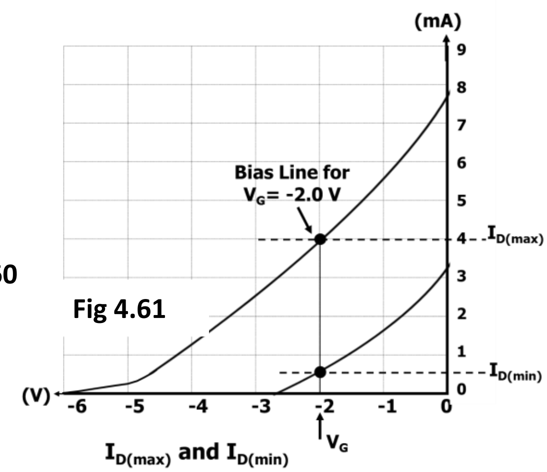


Fig 4.61

Therefore, $I_{D(max)}$ = 4 mA $I_{D(max)}$ = 0.5 mA
$V_{DS(min)} = V_{DD} – I_{D(max)}R_1$ = 25 – (4 mA × 4k) = 9V
$V_{DS(max)} = V_{DD} – I_{D(min)}R_1$ = 25 – (0.5 mA × 4k) = 23V

Note: Gate bias technique has a limited usage. If a FET is replaced by different FET type all the above values will change.

Gate bias – p-channel JFET

Circuit configurations are shown using $-V_{DD}$ and $+V_{DD}$

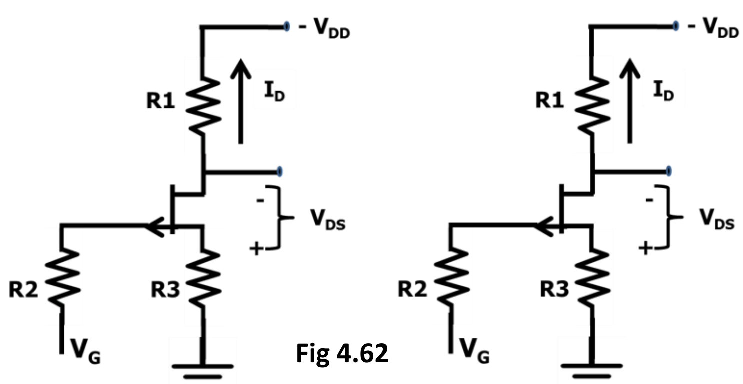


Fig 4.62

Analysis is similar to nJFET.

4.25 FET self bias :

Fig 4.63 shows an nJFET self bias circuit

R_1 is a drain resistor from Drain connected to $+V_{DD}$

R_2 is a gate bias resistor connected between gate and ground

R_3 is a source resistor connected between source and ground

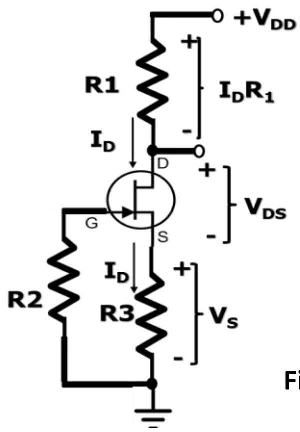


Fig 4.63

The voltage drop across source resistor R_3 is $V_S = I_D R_3$

If I_D= 0.5mA and R_3 = 2k, then V_S = 1V

What is the V_{GS} bias like ?

Voltage at source is +1V

Voltage at gate is 0V (Why? Because there is negligible gate current through the gate resistor R_2)

$\therefore V_{GS}$ is reverse biased to an extent of 1V. V_{GS} = -1V

Or $V_{GS} = -V_S = -I_D R_3$

Feedback effect : This biasing arrangement is an excellent feedback network.

If I_D tends to increase, V_S increases.

Because V_S increase, the reverse bias V_{GS} (= $-V_S$) increases and opposes the tendency of I_D to increase.

Self bias analysis :

Transfer characteristics help us in analysis of a self-bias JFET circuit

Bias lines are drawn in the case of self bias too. But they are not vertical lines as in the case of gate bias.

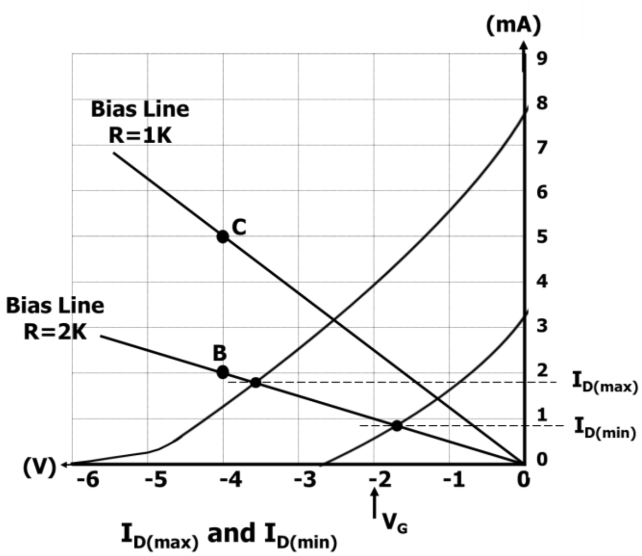


Fig 4.64

We know V_{GS} = -$I_D R_3$
Let us assume R_3 = 2K. and V_{GS} = -4V
∴ I_D = 2mA
Let us plot point B with coordinates (-4,2)
When I_D = 0, V_{GS}= 0. Origin A will be the other point
Join AB which is the bias line for R_3 = 2K.
Similarly for another value of R3 = 1K, V_{GS} = -4, I_D = 4mA and we can plot C as (-4,4)
Let us find I_{Dmax} , I_{Dmin}, $V_{DS(max)}$ and $V_{DS(min)}$ for R_3 = 2k in our example.
Line AB which is a bias line for R_3 = 2k cuts the "minimum and maximum" transfer characteristics at I_{Dmax} = 1.8mA and I_{Dmin} at 0.9mA
We know V_{DD} = $I_D R_1$ + V_{DS} + $I_D R_3$
20V = 1.8mA × 3k + V_{DS} + 1.8mA × 2k
V_{DSmin} = 20 - 5.4 - 3.6
= 11V
V_{DSmax} = 20V - 0.9mA × 3k - 0.9mA × 2k
= 20V - 4.5V
= 15.5V
Similarly, the values of I_{Dmax} , I_{Dmin}, $V_{DS(max)}$ and $V_{DS(min)}$ for R3 = 1K can also be found out.

Self-bias for p-channel JFET :
Refer fig 4.65
Note:
Gate is returned to +V_{DD} through R2
Source is returned to +V_{DD} through R3
Drain is returned to GND through R1
Find I_{Dmax} and I_{Dmin} of the circuit in Fig 4.65 with R1+ 3K and R2=1M and R3 =1K. This is left to the reader.

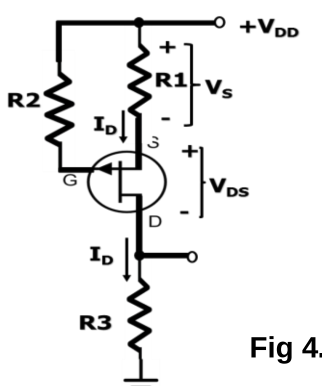


Fig 4.65

The analysis is exactly similar to that of nJFET, otherwise.

4.26 Voltage divider bias-JFET
We had seen in self bias analysis, increasing R_S brings $I_{D(max)}$ and $I_{D(min)}$ closer together. Not only that the absolute values of I_D also get lowered.

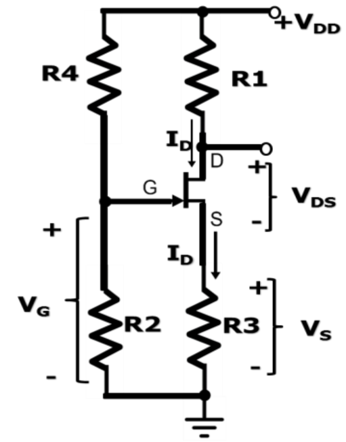


Fig 4.66

Figure 4.66 shows a voltage divider bias circuit. It is similar to that of BJT except that there is no specific base-emitter junction in FET with a drop of 0.7V

Gate bias V_G is determined by R1,R2 junction. Source voltage V_S is determined by R3 and I_D.

$V_{GS}=V_G-V_S$

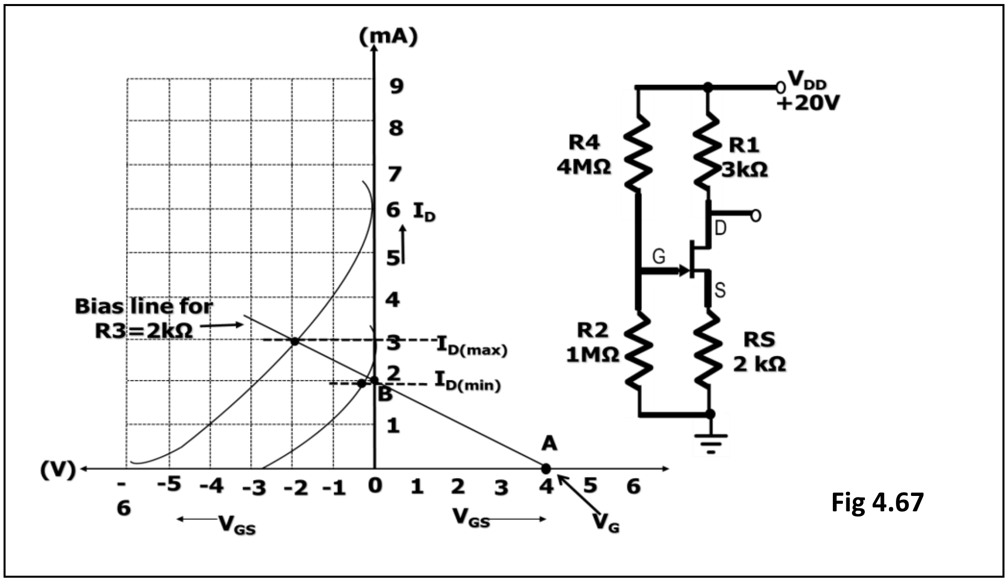


Fig 4.67

Voltage Divider analysis

A FET circuit is shown in fig. 4.67. Let us analyse its operation using the transfer characteristics.

Let us find out $I_{D(max)}$, $I_{D(min)}$, $V_{D(max)}$ and $V_{D(min)}$

$V_G= \frac{\text{VDD } X\ R2}{\text{R2+R4}} = \frac{20\text{V } X\ 1M}{\text{1M+4M}}$ =4V

Case 1:

When I_D=0, $V_{GS}=V_G-I_DR_3$

=4V

Plot A at I_D=0 and V_{GS}=4V

Case-2:

When V_{GS}=0, $\text{ID} = \frac{\text{VG}}{\text{R3}} = \frac{4\text{V}}{2\text{K}}$=2mA

Plot B with I_D=2mA and V_{GS}=0v

Draw the line AB which is the bias line for R3=2K

It intersects the transfer characteristics at $I_{D(max)}$=3.0mA, $I_{D(min)}$=1.9mA

We know $V_{DS(min)}= V_{DD}- I_{DD(max)}(R1+R3)$

$= 20V-3.0mA(3K+2K)$
$= 5V$
$V_{DS(max)} = V_{DD} - I_{DD(min)}(R1+R3)$
$= 20v-1.9mA(3K+2K)$
$= 11.5V$

Voltage divider bias for p-channel FET

Refer Fig 4.68

Gate is returned to $+V_{DD}$ through R4

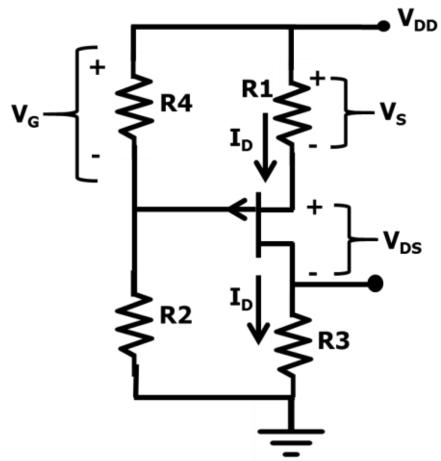
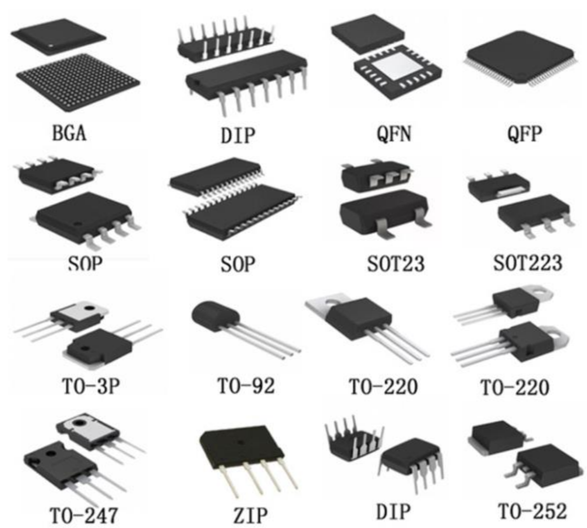


Fig 4.68

Source is returned to $+V_{SS}$ (GND) through R3
Drain is returned to $+V_{DD}$ through R1
The voltage divider resistors are R2 and R4. The analysis is similar to n JFET otherwise.

Chapter 5 Operational Amplifier (Op-Amp)

What is an integrated circuit (IC)?
IC is an electronic circuit formed on a small piece of semiconducting material, normally silicon, which performs the same function as a larger circuit made from discrete components. The integration of large numbers of tiny transistors into a small chip results in circuits that are orders of magnitude smaller, cheaper, and faster than those constructed of discrete electronic components



5.1 Introduction to operational amplifiers

What is an Operational Amplifier?

- Op-amp is the most important analog component. It has two inputs terminals and one output.
- It is an amplifier with high gain and high input impedance (usually with external feedback), used especially in circuits for performing mathematical operations on an input voltage.
- The input terminals are called **non- inverting (+)** and **inverting (–).**
- It is a **high gain** direct coupled (dc) amplifier.
- The operational amplifier works on a dual supply (V+ and V-). There will be a common ground.
- The op-amp has a **huge gain A** (of the order of 10000).
- An **Operational Amplifier**, or op-amp for short, is fundamentally a voltage amplifying device designed to be used with external feedback components such as resistors and capacitors between its output and input terminals.
- The **magnitude of difference between non –inverting and inverting voltage is called differential input V_d**
- Output of op amp = $V_{out} = A \times V_d$
  = $A.(V_{non\text{-}inv} - V_{inv})$

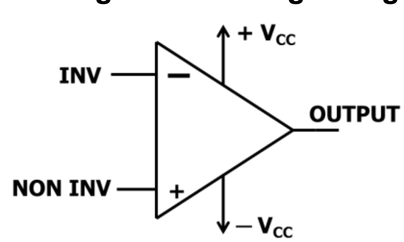


Fig 5.1 Operational Amplifier Circuit symbol

What is the circuit symbol?
Refer Fig 5.1 for circuit symbol.
Abbreviations:
We shall use the following abbreviations in this chapter.

Operational amplifier → op-amp
Inverting → inv
Non- Inverting → non-inv

What is a differential amplifier? What is an inverting amplifier?

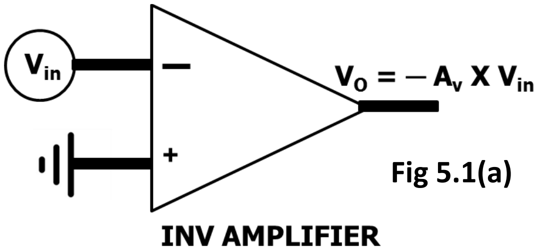


Fig 5.1(a)

In Inverting amplifier, the output waveform is inverted with respect to the input. (Opposite phase). Refer fig 5.3.

- Note that in inverting amplifier configuration, the non-inverting (+) input is grounded.
- Output $V_o = -A_v V_{in}$
- A_v – Gain of the op amp.

What is a non-inverting amplifier?

In the Non-Inverting amplifier, the output waveform is in the same phase with respect to the input. There is no inversion. Refer fig 5.4

Op amp terminals and Packages

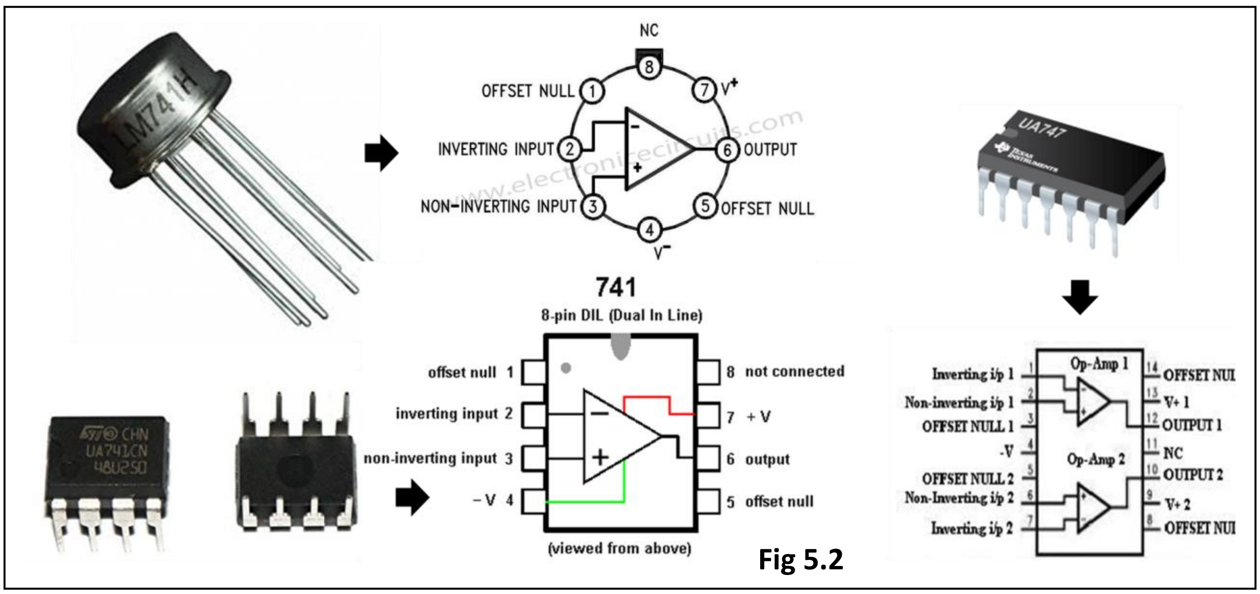


Fig 5.2

Popular Op amp: 741 , 747 is a dual 741

Op amp Power supply connections

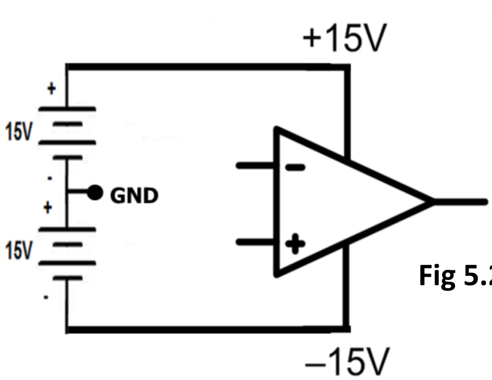


Fig 5.2 (a)

The **µA741** op-amp is a general-purpose op-amp with a **BJT** input stage. It is capable of producing output voltages of **±14V** with DC power supply voltages of **±15V**.
The parameters are
$R_i = 2M\Omega$, $R_o = 75\Omega$, $A_o = 2\times10^5$,
Break frequency $f_b = 10Hz$,
and **unity-gain bandwidth** $f_{bw} = 1MHz$.

In reality what do you get in Op amps?

What You WANT	What You GET
1) The input impedance is infinite - i.e. no current ever flows into either input of the op-amp.	NO, but it is often GIGA or TERA Ω!
2) The output impedance is zero - i.e. the op-amp can drive any load impedance to any voltage.	NO, but is can be a few ohms in many cases!
3) The open-loop gain (A) is infinte.	NO, but it is usually several million!
4) The bandwidth is infinite.	NO, usually several MHz.
5) The output voltage is zero when the input voltage difference is zero.	NO, offset voltages exist, but can be trimmed.

What is the differential input concept?

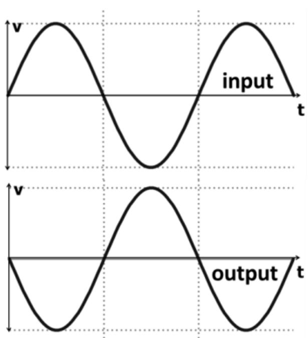


Fig 5.3 Inverting amplifier Input/Output waveforms

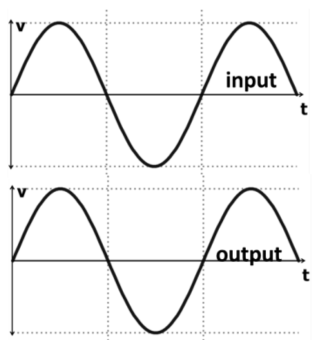


Fig 5.4 non-inverting amplifier Input/Output waveforms

Refer fig 5.4 (a) and 5.5. The op-amp always amplifies the difference between the inv and non-inv inputs.
V_d is the difference between the voltages present at inv and non-inv terminals.

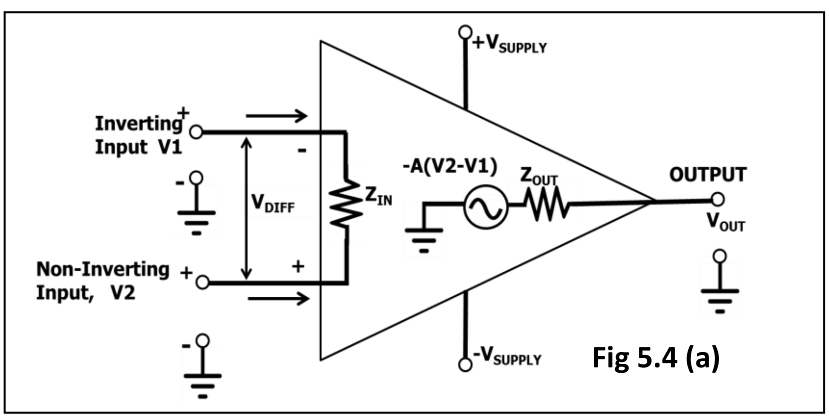


Fig 5.4 (a)

V_d = V2 – V1 (Differential voltage)
Output will be V_d X Gain of the op-amp (A).
$V_o = V_d$ X A.
For an ideal op-amp gain A = ∞.

$$\therefore V_d = V2 - V1 = \frac{V_O}{A} = \frac{V_O}{\infty} = \mathbf{0}$$

∴ There are two interesting conclusions here.

1. **For an op-amp, the <u>differential voltage = 0</u>**
2. **For an op-amp, <u>Inverting and Non-Inverting terminals will be at the same potential. They follow each other</u>**

What is the virtual ground in an op-amp?

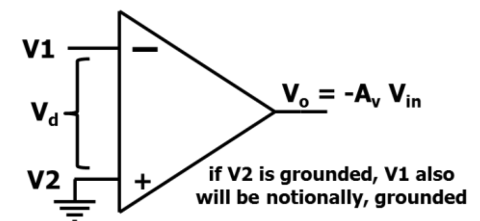


Fig 5.5 Virtual Ground

This is applicable to inverting amplifiers. Virtual ground means that if V2 is grounded, V1 also will be at ground potential (0 V). Therefore **notionally, V1 also is grounded even if there is no physical connection to ground**. V1 is said to be **virtually grounded**.

Differential Amplifier

What is a differential amplifier?

A **differential amplifier** is a circuit that can accept two input signals and amplify the difference between these two input signals

A simple differential amplifier with two inputs marked V_1 and V_2 is shown. TR_1 and TR_2 are identical transistors and they are both biased at the same operating point with their emitters connected together and returned to the common –ve power supply, $-V_{EE}$ through resistor R_E.

The circuit operates from a dual supply +Vcc and $-V_{EE.}$ The output voltage V_{out} is the difference between the two input signals as the two base inputs are in anti-phase with each other.So as the forward bias of transistor, TR_1 is increased, the forward bias of transistor TR_2 is reduced and vice versa. **Why?**

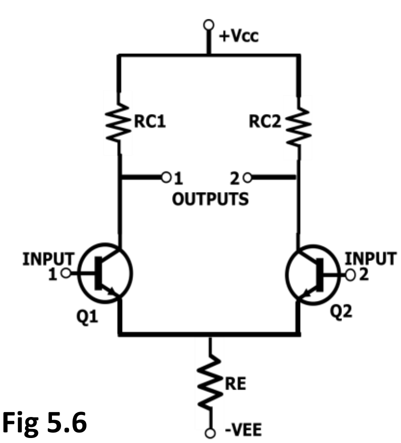


Fig 5.6

If signal V_1 at TR_1 base voltage is increased, the junction of TR_1 emitter, TR_2 emitter and resistor R_E also rises (simply follows V_1). If V_2 is at a a constant potential, the bias voltage across TR_2 base emitter decrease. Then if the two transistors are perfectly matched, the current flowing through the common emitter resistor, R_E will remain constant

Common Mode of Operation : Assume V1 and V2 are exactly identical, Assume the characteristics of both the transistors are also identical. Therefore the collector voltages of each transistor will be at the same value. The output voltage signal V_{out}, is taken between the two collectors and therefore V_{out} will be zero.

The **common mode gain** of the amplifier is the output gain when the input is zero.

Fig.5.7 a shows the block diagram of an ordinary amplifier. The input voltage v is amplified to Av where A is the voltage gain of the amplifier. Therefore, the ouput voltage is v_0 = Av.

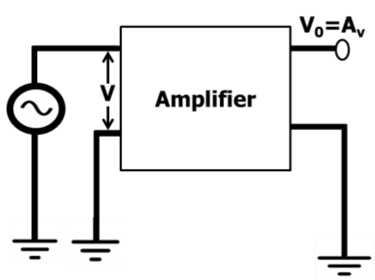


Fig 5.7 (a)

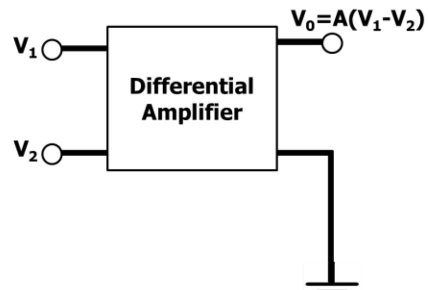


Fig 5.7 (b)

Fig. 5.7 b shows the block diagram of a differential amplifier. There are two input voltages v_1 and v_2. This amplifier amplifies the difference between the two input voltages. Therefore, the output voltage is v0 = A(v1 – v2) where A is the voltage gain of the amplifier.

Example 1. A differential amplifier has an open-circuit voltage gain of 200. The input signals are 3.5 V and 3.4 V. Determine the output voltage.
Output voltage, v0 = A(v1 – v2), Here, A = 200 ; v1 = 3.5 V : v2 = 3.4V
∴ v0 = 200(3.5 – 3.4) = **20V**

Basic Circuit of Differential Amplifier

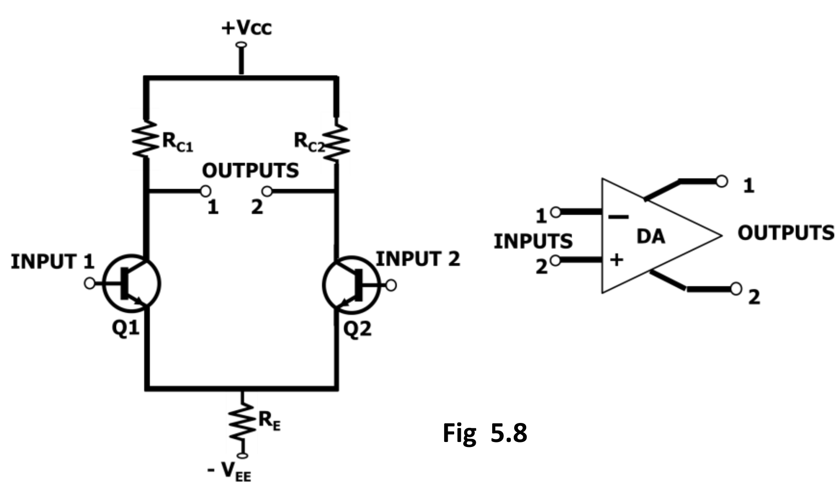


Fig 5.8

Fig. 5.8   shows the basic circuit of a differential amplifier. It consists of two transistors Q1 and Q2 that have identical characteristics. V_{CC} and V_{EE} are the positive and negative supplies. Differential amplifier is a symmetrical circuit.

Note,

The differential amplifier (DA) is a two-input terminal device and a two output terminals (vout 1 and vout 2).

Resistors RC1 and RC) are also equal.

Input methods:

(a) Single-ended input : The signal can be applied to just one input and the other input is grounded.

(b) Dual-ended or double-ended input: The signals are applied to both inputs of DA.

Output methods:

(a) Single-ended output: Output is taken from one of the output terminals and the other output is grounded.

(b) Double-ended output: Output is taken between the two output terminals (i.e., between the collectors of Q1 and Q2).

In general, the differential amplifier is operated for single-ended output.

Operation of Differential Amplifier

Assume the signal is applied to input 1 (i.e., base of transistor Q1) and input 2 (i.e., base of transistor Q2) is grounded as shown in Fig,

The input signal at transistor Q1 will appear at output 1(collector of Q1) as amplified and inverted.

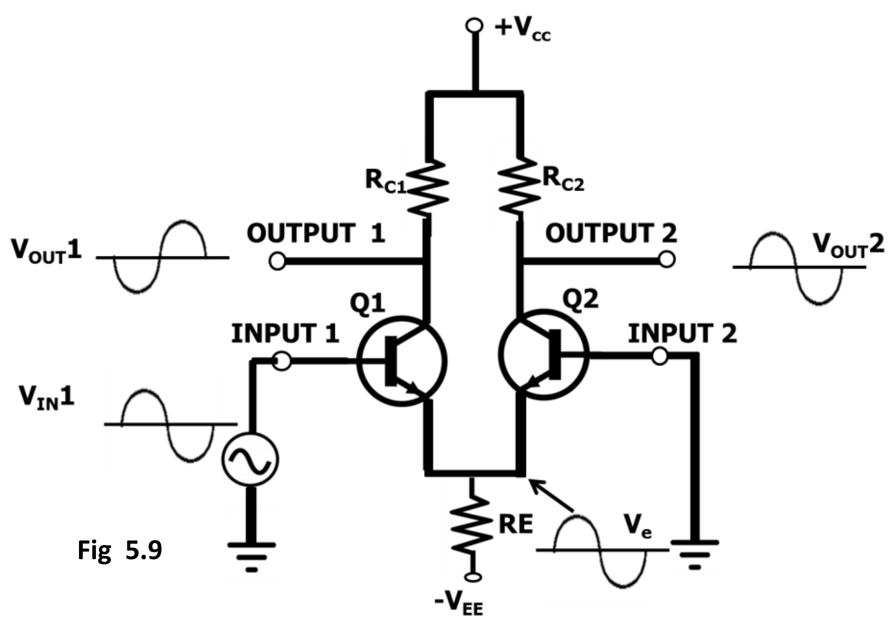


Fig 5.9

The input signal at transistor Q1, also appears on the emitter of Q1 in phase with the input and slightly attenuated.

The emitters of Q1 and Q2 are common and therefore, the emitter signal becomes input to Q2. You can see, Q2 functions as a *common base amplifier.
Therefore, the signal on the emitter of Q2 will be amplified and appears on output 2 (collector of Q2) in phase with the emitter signal and hence in phase with the input signal (signal at input 1).

This is illustrated in Fig 5.9.

Alternatively if the signal is applied to input 2, the roles of Q1 and Q2 are reversed. Q2 acts as a common emitter amplifier while Q1 functions as a common base amplifier. This is shown in the figure 5.10 below.

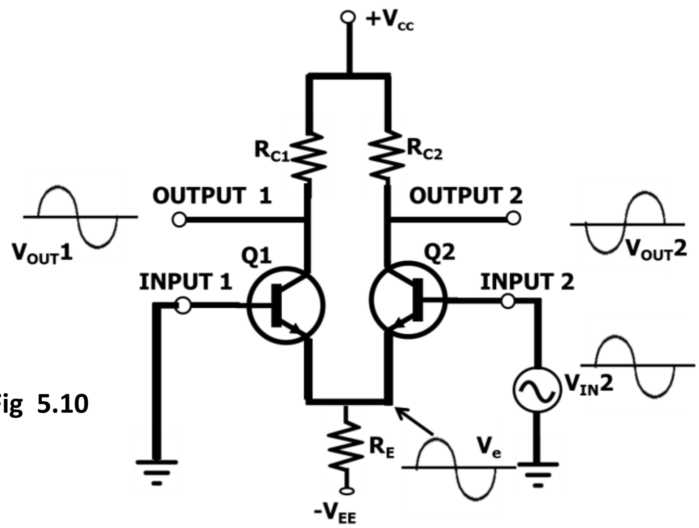


Fig 5.10

What is happening here?
When signal is applied to input 1 and input 2 is grounded, an inverted signal appears at output 1 and non-inverted signal appears at output 2.
When signal is applied to input 2 and input 1 is grounded, an inverted signal appears at output 2 and non-inverted signal appears at output 1.
This is shown in figure 5.11 below

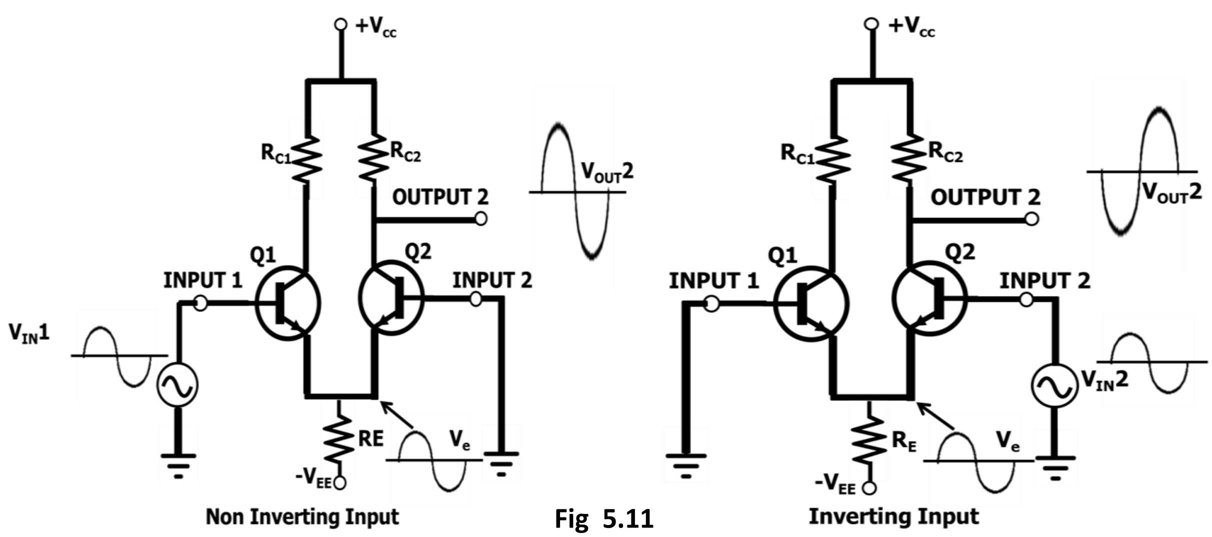


Fig 5.11

When signal applied to the input of DA produces no phase shift in the output, it is called noninverting input [See Fig].

- In other words, for noninverting input, the output signal is in phase with the input signal. The noninverting input is then represented by +*sign.
- When the signal applied to the input of DA produces 180° phase shift, it is called inverting input [See Fig].
- In other words, for inverting input, the output signal is 180° out of phase with the input signal.It is often identified with –sign.

Note that in Fig.5.11, the noninverting input terminal is given the +ve sign while the inverting input terminal is given the –ve sign.

It may be noted that terms noninverting input and inverting input are meaningful when only one output terminal of DA is available.

Common-mode and Differential-mode Signals

In a differential amplifier, the outputs are proportional to the difference between the two input signals. Thus the circuit can be used to amplify the difference between the two input signals or amplify only one input signal simply by grounding the other input.

The **input signals to a DA** can be of two types.
(i) Common-mode signals (ii) Differential-mode signals

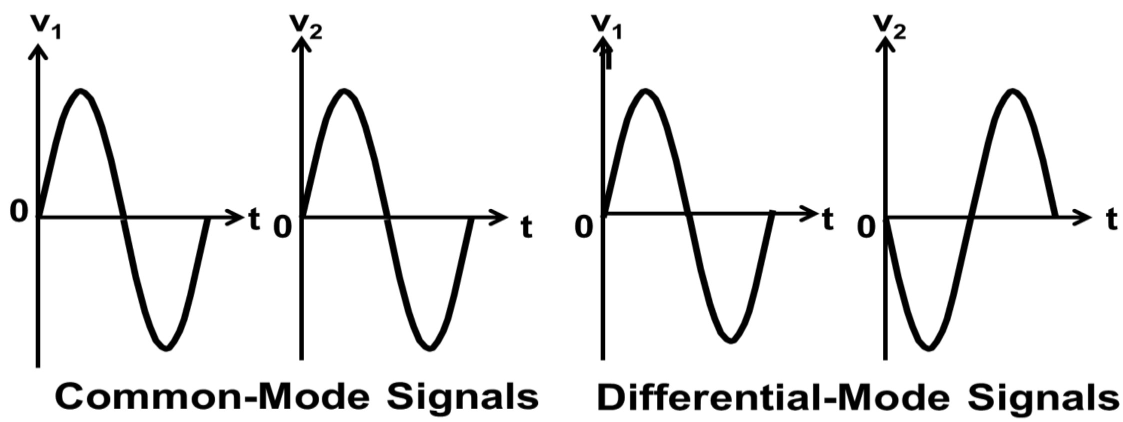


Fig 5.12

(i) Common-mode signals : When the **input signals to a DA are in phase and exactly equal in amplitude,** they are called common-mode signals as shown in Fig 5.12.

The common-mode signals are rejected (not amplified) by the differential amplifier. It is because a differential amplifier amplifies the difference between the two signals (v1 – v2) and for common-mode signals, this difference is zero. Note that for common-mode operations, v1 = v2.

(ii) Differential-mode signals. When the **input signals to a DA are 180° out of phase and exactly equal in amplitude,** they are called differential-mode signals as shown in Fig 5.12.

The differential-mode signals are amplified by the differential amplifier. It is because the

difference in the signals is twice the value of each signal. For differential-mode signals, v1 = –v2.

Thus we arrive at a very important conclusion that a differential amplifier will amplify the differential-mode signals while it will reject the common-mode signals.

6. Voltage Gains of DA

The voltage gain of a DA operating in differential mode is called differential-mode voltage gain and is denoted by ADM.

The voltage gain of DA operating in common-mode is called common-mode voltage gain and is denoted by ACM.

Ideally, a DA provides infinite voltage gain for differential-mode signals and zero gain for common-mode signals.

But, in practice, it does not happen. At best differential voltage gain will be very high of the order of several thousands and common-mode gain will be very small, usually much less than 1 but not zero.

The op amp will have a high figure of merit if the ratio of differential gain to. the common-mode gain is very high.

7 Common-mode Rejection Ratio (CMRR)

A differential amplifier should have high differential voltage gain (ADM) and very low common-mode voltage gain (ACM).
The ratio ADM/ACM is called common-mode rejection ratio (CMRR)

$$\text{CMRR} = \frac{A_{DM}}{A_{CM}}$$

Very often, the CMRR is expressed in decibels (dB). The decibel measure for CMRR is given by;

$$\text{CMRR}_{dB} = 20\log_{10}\frac{A_{DM}}{A_{CM}} = 20\log_{10}\text{CMRR}$$

The following table shows the relation between the two measurements :

CMRR	CMRR_{dB}
10	20dB
10^3	60dB
10^5	100dB
10^7	140dB

Importance of CMRR. The CMRR is the ability of a DA to reject the common-mode signals. The larger the CMRR, the better the DA is at eliminating common-mode signals.

Let us illustrate this point.
Suppose the differential amplifier in Fig has a differential voltage gain of 1500 (i.e., ADM = 1500) and a common-mode gain of 0.01 (i.e., ACM = 0.01).

CMRR = 1500/0.01 = 150,000

Why high CMRR?
Common-mode signals are usually undesired signals caused by external interference.
For example, any RF signals or noise picked up by the DA inputs would be considered undesirable.
The CMRR indicates the DA's ability to reject such unwanted signals.

Example 2. A certain differential amplifier has a differential voltage gain of 1000 and a common mode gain of 0.1.What is CMRR and express it in dB.

Solution. CMRR = ADM/ ACM = 1000/ 0.1 = **10,000**
CMRRdB = 20 $\log_{10}$ 10,000 = **80dB**

Example 3. A differential amplifier has an output of 2V with a differential input of 10 mV and an output of 2,5 mV with a common-mode input of 10 mV. Find the CMRR in dB.

Solution.
Differential gain, ADM = 2V/10 mV = 200
Common-mode gain, ACM = 2.5 mV/10 mV =0.25
∴ CMRRdB = 20 log10 (200/0.25) = **49 dB**

Example 4.
A differential amplifier with a CMRR of 80 dB.has a voltage gain of 200. The input signals are 150 mV and 200 mV with 1 mV of noise on each input. Find (i) the output signal (ii) the noise on the output.

Solution.
(i) Output signal, vout = ADM(v1 – v2) = 200 (200 mV –150 mV) = 10 **V**
(ii) $CMRR_{dB}$ = 20 log10 (200/ACM)
or 80 = 20 log10 (200/ACM)
∴ ACM = 20×10^{-3}
Noise on output = ACM × 1 mV = 20×10^{-3} × 1mV = 20 × $\mathbf{10^{-6}}$ **V**

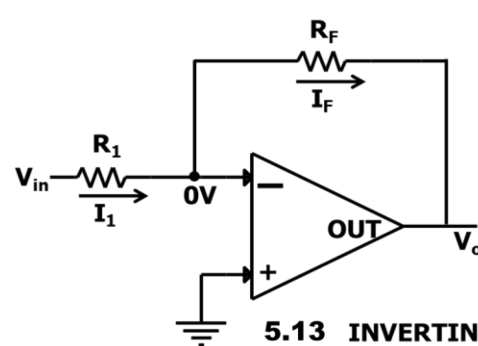
5.2 Inverting Amplifiers

Derive an expression for gain of an inverting amplifier (Fig 5.13).

- Input is fed to the Inverting (—) terminal.
- Non-inv (+) is grounded.
- Therefore, Inv input = 0 V (Virtual ground).
- The op-amp input terminals never draw any input current.
- Therefore, the entire input current I_1 flows into the feedback circuit as I_F. Therefore $I_1 = I_F$

$$\frac{V_{IN} - 0}{R_1} = \frac{0 - V_O}{R_F} \rightarrow \frac{V_{IN}}{R_1} = \frac{-V_O}{R_F}$$

Therefore, $\frac{V_O}{V_{IN}} = -\frac{R_F}{R_1}$



5.13 INVERTING AMPLIFIER

What are the important aspects to be understood, in op amp circuits ?

Note 1: If non- inverting input is grounded, inverting input also will be at ground potential. This concept is called **virtual ground** (Inv input will be at ground potential without any physical connection to ground).

Note 2: If inverting input is at a potential V1, the non – inverting input also be at V1**. ("Non-inv" will follow "inv").**

Note 3: From both (1) and (2), it can be inferred, that inverting and non – inverting inputs follow each other. The difference between "inv" and "non-inv" inputs is called differential voltage and is denoted by V_d. ($V_d = V_+ - V_-$) $\mathbf{V_d}$ **in an op-amp is always zero**.

Note 4: The current drawn by the inverting input terminal or the non- inverting input terminal is zero. Therefore, in op amp analysis **current drawn by V+ pin or V— pin can be neglected**.

Problem 1: For the op-amp in fig 5.14, the input is a sinewave of I Volt, I kHz. What is the output?

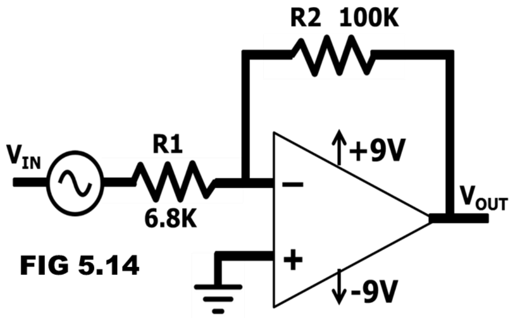


FIG 5.14

For non-inverting amplifier, $\mathbf{V_{out} = -V_{in}\ \frac{R_2}{R_1}}$

In this problem, frequency does not matter.

V_{in} = I Volt. **[I V is rms (by default)]**

V_{in} = I V rms = 1 V X $\sqrt{2}$ = 1.4 V peak.(just one peak)

= ± 1.4 V peak (both peaks)

V_{out} = ± 1.4 V X $\frac{\mathbf{100K}}{\mathbf{6.8K}}$ = ± 11.8 V peak .

Positive peak is 11.8 V and negative peak is - 11.8 V

This is not possible since the op amp has a DC supply of +9 V and –9 V. Therefore the peaks will clip at the power supply voltages.

The input / output waveforms are shown in fig 5.15

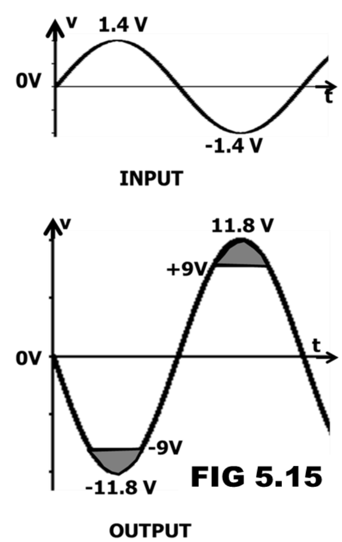


FIG 5.15

Problem 2: What is the input current and load current for this op-amp shown in fig 5.16?

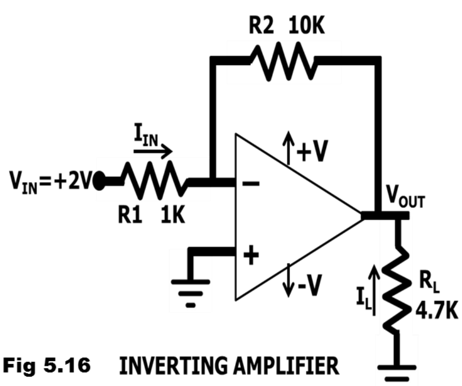


Fig 5.16 INVERTING AMPLIFIER

The inv input terminal is at 0 V **(virtual ground)**.

Input current $= \frac{2\text{ V} - 0\text{ V}}{1\text{K}}$ = 2 mA

V_{out} $= -V_{in}\frac{\text{R2}}{\text{R1}}$ $= -\ 2 \text{ X } \frac{10\text{K}}{2\text{K}}$ $= -\ 10\text{V}$

Load current $= I_L \frac{V_{out}}{R_L} = \frac{-10\text{ V}}{4.7\text{K}} = -2.5\text{ mA}$

I_L is – ve. ∴current flows from ground thro R_L, into the op amp, as shown in the circuit diagram 516. The waveform is shown in **fig 5.15**.

Problem 3: What is V_O for the op-amp in fig 5.17?

This is an inverting amplifier.

Therefore $\frac{V_O}{V_{IN}} = -\frac{R_F}{R_1}$

Gain $= -\frac{V_O}{V_{IN}} = -\frac{100K}{10\text{ K}} = -10$

∴ $V_o = -10 \times 0.6\text{ V} = -6\text{ V}$

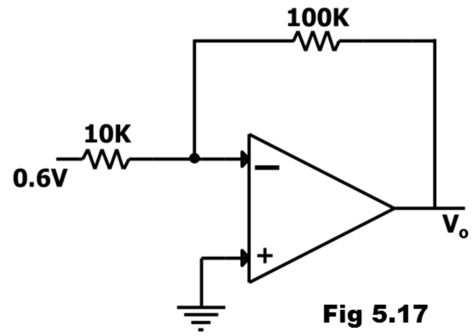


Fig 5.17

5.3 Non-inverting amplifier

Derive an expression for gain of a non-inverting (+) amplifier.

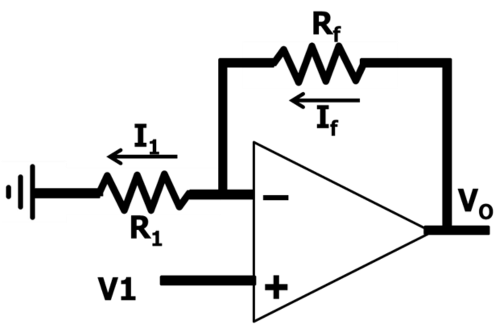


Fig 5.18 . NON-INV AMPLIFIER

- Refer **fig 5.18.**
- Note that **the feedback is always between the V_o and Inv terminal**.
- Input is now fed at non-inv (+) terminal.
- **R_1 is grounded**.
- Note that Inv terminal (—) also is **at V_1.** (Both inv and non inv terminals will be at the same potential and **follow each other**)
- No current flows into inv (—) terminal.
- Therefore, the entire current I_F flows into the input resistor as I_1

Therefore $I_1 = I_F$

$$\frac{V_O - V_1}{R_F} = \frac{V_1 - 0}{R_1}$$

$$\frac{V_O}{R_F} = \frac{V_1}{R_1} + \frac{V_1}{R_F}$$

$$V_O = V_1\left\{\frac{R_F}{R_1} + 1\right\}$$

$$= V_1\left\{1 + \frac{R_F}{R_1}\right\}$$

Therefore, Gain $= \frac{V_O}{V_1} = \left\{1 + \frac{R_F}{R_1}\right\}$

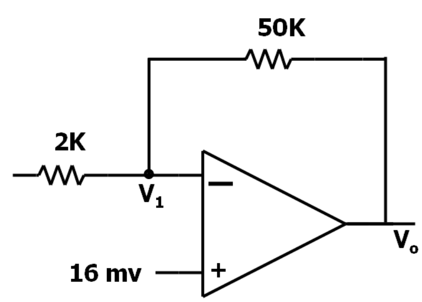


Fig 5.19

Problem 4: For the circuit in fig 5.19, V_o = ? Gain = ?

This is a non-inverting amplifier.

Gain $= \frac{V_O}{V_1} = \left\{1 + \frac{R_F}{R_1}\right\}$

$= \left(1 + \frac{50\text{ K}}{2\text{ K}}\right) = 26$

$V_o = V_{in}\left\{1 + \frac{R_F}{R_1}\right\}$

= 16 X 26 =416 mV

Problem 5: For the circuit in fig 5.20, what is V_O? What is the load current?

First, determine the voltage at B. Note the voltage at B IS NOT 2.2 V but a potential division of 1K and 1.2 K.

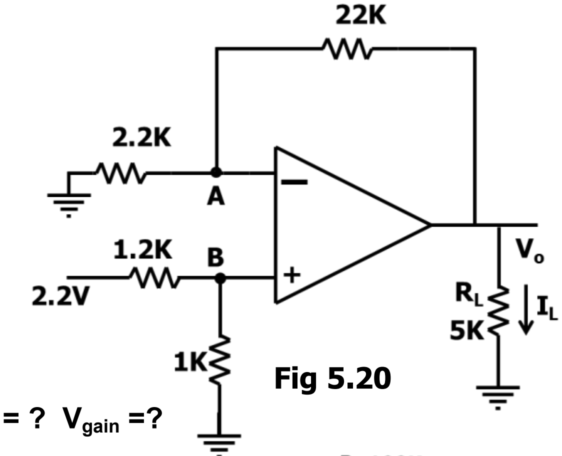


Fig 5.20

$V_B = \frac{2.2\ V\ X\ 1\ K}{1K+1.2\ K} = 1.0\ V$

$V_O \quad = V_B\ (1 + \frac{R_F}{R_{in}})$

$= 1.0\ V\ (1 + \frac{22\ K}{2.2\ K})$

$= 1.0\ V\ X\ 11 \quad = +11\ V.$ (Non-Inverting)

Problem 6: In the circuit shown in fig 5.21, V_{out} = ? V_{gain} =?

$V_{out} = V_{in}\ (1+ \frac{R_f}{R_{in}})$

What is V_{in}? Note V_{in} is NOT 5 V .

It will be the actual voltage V_{in} at the non-inverting (+) terminal, after a potential division by R1 and R2.

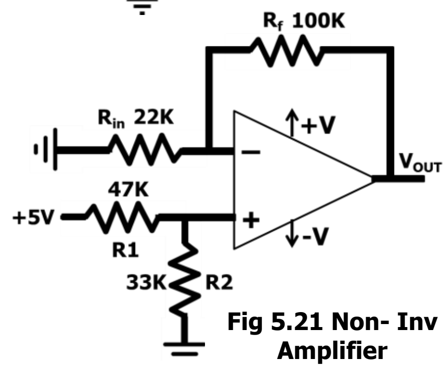


Fig 5.21 Non- Inv Amplifier

$V_{in} \ = 5\ V \frac{R2}{R1+R2} \ = 5\ V\ X \frac{33K}{33K + 47K} \ = 2.1\ V$

$V_{out} \ = V_{in}\ (1 + \frac{R_f}{R_{in}}) \ = 2.1\ V\ (1 + \frac{100K}{22K}) \ = 11.65\ V$

$V_{gain} = \frac{V_{out}}{V_{in}} \ = \frac{11.65V}{5V} \ = 2.33$

5.4 Summing Amplifiers

Non inverting summing amplifier (Refer fig 5.22)

It is a non-inverting amplifier . Therefore $V_{out} = V_3\ (\mathbf{1} + \frac{R_f}{R_{in}})$

How to find V_3 ?

At the non-inv terminal, I_1 flows through R1 and I_2 flows through R2, but the input current I_{in} to the non- inverting (+) terminal = 0

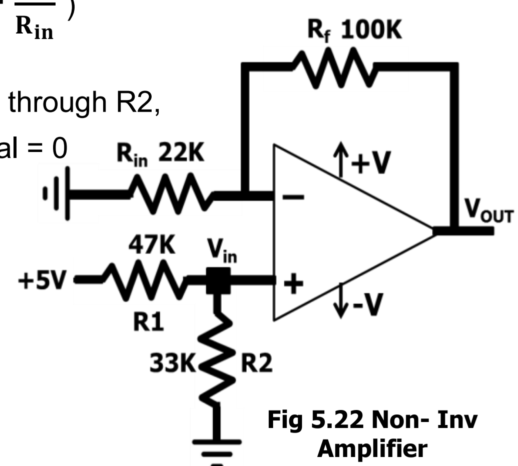


Fig 5.22 Non- Inv Amplifier

$\therefore I_1 + I_2 = 0$

$\therefore \ \frac{V_1 - V_3}{R_1} + \frac{V_2 - V_3}{R_2} = 0$

$\frac{V_1}{R_1} + \frac{V_2}{R_2} = \frac{V_3}{R_1} + \frac{V_3}{R_2} \ = V_3 \left(\frac{1}{R_1} + \frac{1`}{R_2}\right)$

$\frac{V_1 R_2 + V_2 R_1}{R_1 R_2} = V_3 \left(\frac{R_2 + R_1}{R_1 R_2} \right)$

or $\quad V_3 = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}$

$V_{out} \ = \ V3 \left(1 + \frac{R_f}{R_{in}}\right)$ [non–inv op amp]

$= \left(\frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}\right) \left(1 + \frac{R_f}{R_{in}}\right)$

Case 1: Let $R_1 = R_2$, then $V_{out} = \frac{1}{2} (V_1 + V_2) \left(1 + \frac{R_f}{R_{in}} \right)$

Case 2: Also let $R_f = R_{in}$ then $V_{out} = (V_1 + V_2)$ **[This is a SUMMING AMPLIFIER]**

Derive an expression for an inverting, summing amplifier.

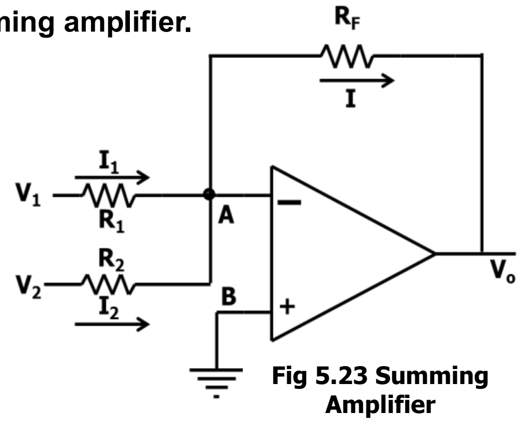


Fig 5.23 Summing Amplifier

Refer fig 5.23. $V_B = 0 \therefore V_A = 0$

$I_1 + I_2 = I$

$I_1 = \frac{V_1 - V_A}{R_1} = \frac{V_1}{R_1}$ (since VA = 0)

$I_2 = \frac{V_2 - V_A}{R_2} = \frac{V_2}{R_2}$ (since VA = 0)

$I = \frac{V_A - V_O}{R_F} = -\frac{V_O}{R_F}$

$I_1 + I_2 = I$

$\frac{V_1}{R_1} + \frac{V_2}{R_2} = -\frac{V_O}{R_F}$

$\therefore V_O = -\left\{ \left(\frac{R_F}{R_1}\right) V_1 + \left(\frac{R_F}{R_2}\right) V_2 \right\}$

Case 1: $R_1 = R_2 = R$ $\quad$ $V_O = -\frac{R_F}{R}(V_1 + V_2)$ **(Summing amplifier)**

Case 2: $R_1 = R_2 = R_F = R$ $\quad$ $V_O = -(V_1 + V_2)$ **(Summing amplifier)**

Case 3: $R_1 = R_2 = R$ and $R_F = (R/2)$ $\quad$ $V_o = -\frac{(V_1+V_2)}{2}$. **(Averaging amplifier.)**

Problem 7: Refer circuit shown in fig 5.24.
What is the output?

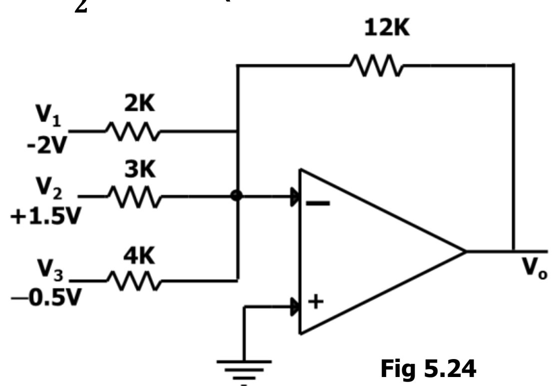


Fig 5.24

$V_O = R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)$

$= 12K \left(\frac{-2\ V}{2K} + \frac{1.5\ V}{3K} - \frac{0.5\ V}{4K}\right)$

$= -12\ V + 6\ V - 1.5\ V.$

$V_O = -7.5\ V$

Summing circuit (adder) using super position

Problem 8 : What is the output of this circuit if V1 = 2 V, V2 = 3 V and V3 = 5 V

Refer fig 5.25. This can be analysed by using super position theorem.

Superposition principle : When one voltage source is connected all other voltage source should be replaced by short. (in this example, to be replaced by ground) .

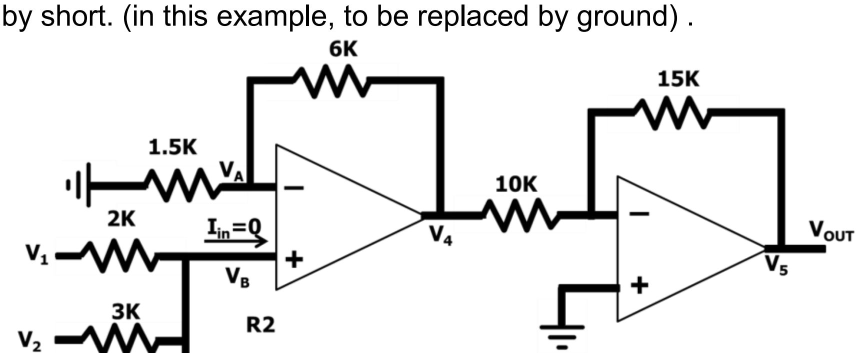


Fig 5.18 Summing circuit (Adder) analysis sing Superposition

Fig 5.25

a) **V1 is connected** (Refer fig 5.26)

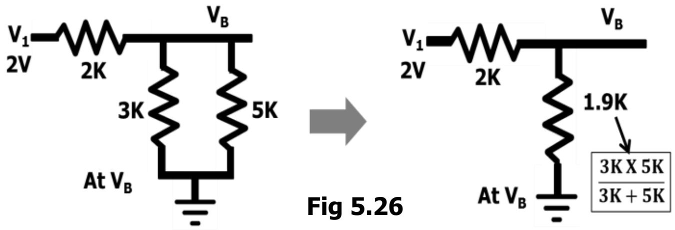


Fig 5.26

$$V_B = \frac{V_1 \text{ X } 1.9K}{2K+1.9K} = \frac{2V \text{ X } 1.9K}{3.9K} = 0.97 \text{ V}$$

$$V_{out} = V_B\left(1 + \frac{R_f}{R_{in}}\right) = 0.97\ (1 + \frac{6K}{2K}) = \mathbf{3.9\ V}$$

b) V_2 is connected (Refer fig 5.27)

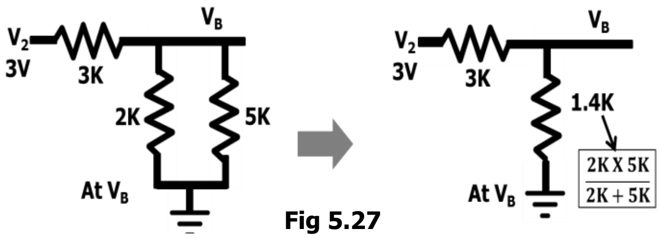


Fig 5.27

$$V_B = \frac{V_2 \text{ X } 1.4K}{3K+1.4K} = \frac{3V \text{ X } 1.4K}{4.4K} = 0.95 \text{ V}$$

$$V_{out} = V_B\left(1+\frac{R_f}{R_{in}}\right) = 0.95\ (1 + \frac{6K}{2K}) = \mathbf{3.8\ V}$$

c) V_3 is connected (Refer fig 5.28)

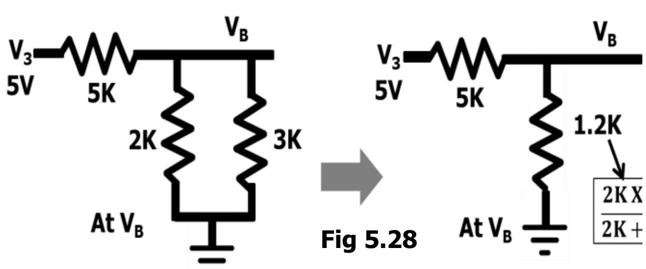


Fig 5.28

$$V_B = \frac{V_3 \text{ X } 1.2K}{5K+1.2K} = \frac{5V \text{ X } 1.2K}{6.2K} = 0.97 \text{ V}$$

$$V_{out} = V_B\left(1+\frac{R_f}{R_{in}}\right) = 0.97\ (1 + \frac{6K}{2K}) = \mathbf{3.9\ V}$$

$\therefore$ the final voltage at adder o/p V_4 = 3.9 + 3.8 + 3.9 = 11.6V

The output at $V_5 = -V_4 \text{ X } \frac{15K}{10K} = -11.6 \text{ X} 1.5 = \mathbf{-17.4\ V}$

5.5 Subtractor

Derive an expression for a subtractor.
Subtractor is also called (Difference Amplifier)

At negative terminal,

$$\frac{V_1 - V'}{R_1} = \frac{V' - V_O}{R_2}$$

$$\frac{V_O}{R_2} = \frac{V'}{R_2} + \frac{V'}{R_1} - \frac{V_1}{R_1}$$

$$= V'\left(\frac{1}{R_2} + \frac{1}{R_1}\right) - \frac{V_1}{R_1} \quad \rightarrow \textbf{(A)}$$

$$V' = V'' = \frac{V_2 R_2}{R_1 + R_2}$$

Substitute for V' in (A)

$$\frac{V_O}{R_2} = \frac{V_2 R_2}{R_1 + R_2}\left(\frac{R_1 + R_2}{R_1 R_2}\right) - \frac{V_1}{R_1}$$

$$\frac{V_O}{R_2} = \frac{V_2}{R_1} - \frac{V_1}{R_1} = \frac{1}{R_1}\ (V_2 - V_1)$$

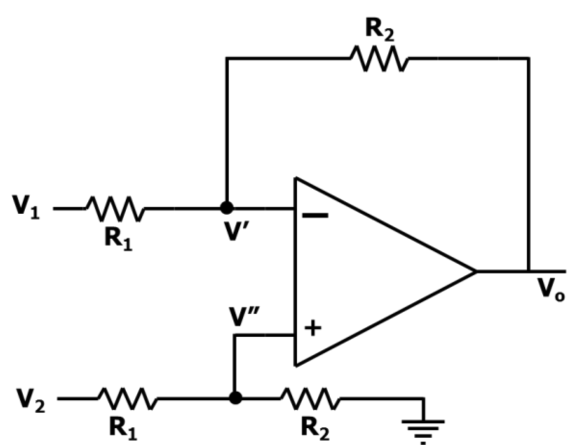


Fig 5.29 SUBTRACTOR

$V_O = \frac{R_2}{R_1}(V_2 - V_1)$

If $R_2 = R_1$, $V_O = (V_2 - V_1)$

This is a subtractor.

Problem 9: Implement this. $V_O = V_1 - 3V_2 - 2V_4 + 5V_3$. Assume R_F = 30 K.

Implementation: Refer fig 5.30. Regroup all +ve terms all –ve terms.. $V_O = (V_1 + 5V_3) - (3V_2 + 2V_4)$

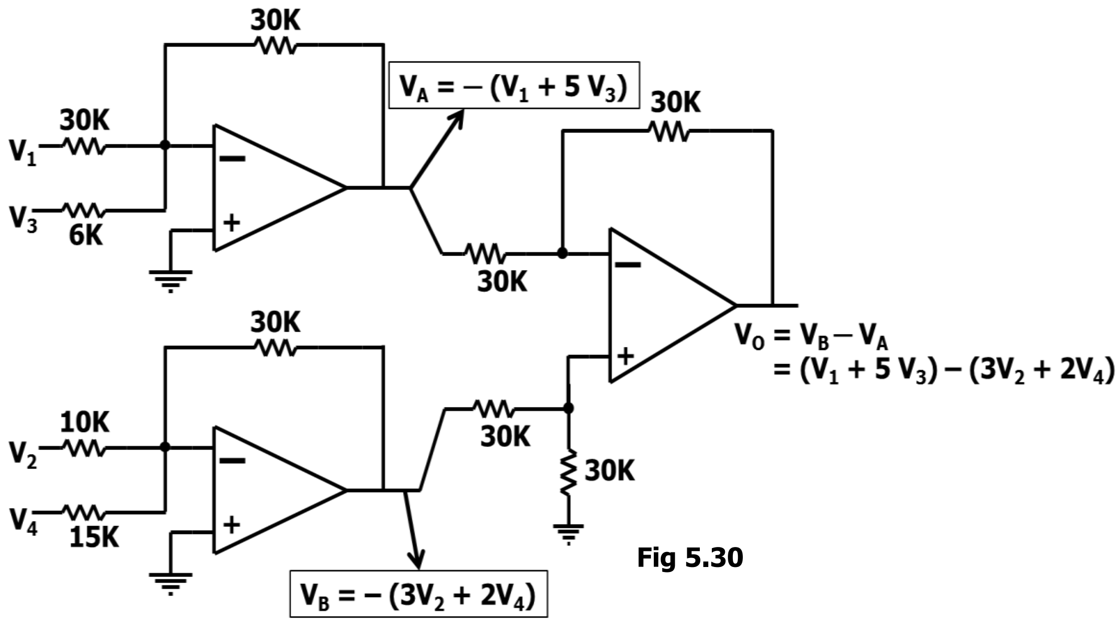


Fig 5.30

Problem 10: This is known as Scaling order. Design a scaling order to give an output $V_O = -(6V_1 - 4V_2 + 3V_3)$. Choose R_F = 120 K. Refer fig 5.31.

Implementation:

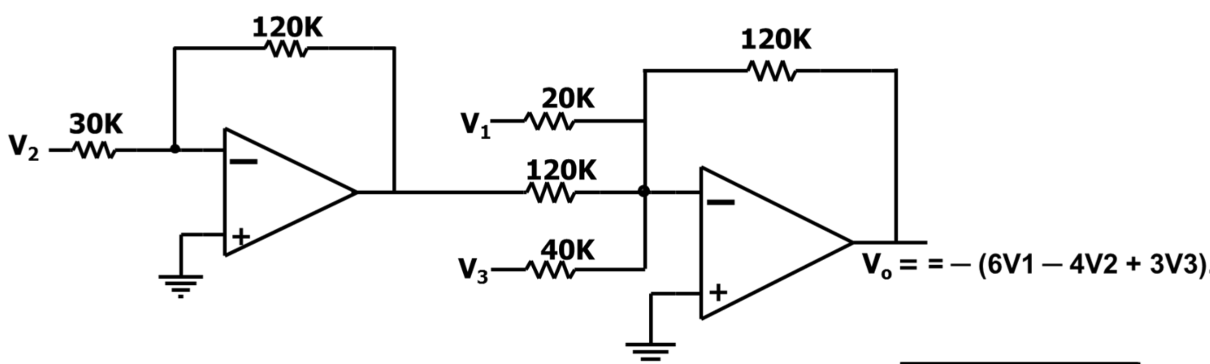


Fig 5.31

5.6 Op-amp applications

5.6.1 Voltage Follower application: (Refer fig 5.32)

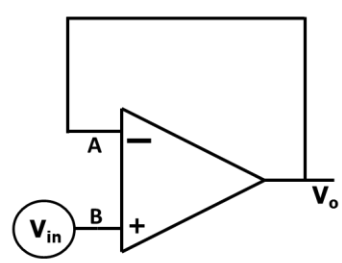


Fig 5.32 VOLTAGE FOLLOWER

Voltage Gain = Unity

$V_B = V_{in}$

$V_A = V_B = V_{in}$

$V_O = V_A = V_B = V_{in}$

$\therefore V_O = V_{in}$

Output follows Input.

Hence the name “**Voltage Follower**”
Voltage Gain = Unity
Large Input impedance
Low output impedance

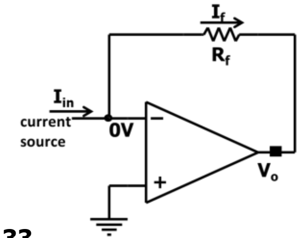


Fig 5.33 CURRENT TO VOLTAGE CONVERTER TRANS RESISITANCE AMPLIFIER

5.6.2 Current to Voltage Converter application – Trans-resistance Amplifier: (Refer fig 5.33)

$I_{in} = I_f$

$I_{in} = \frac{0-V_O}{R_F} = -\frac{V_O}{R_F}$

$\therefore$ I_{in} is proportional to $-$Vo

Input Current is proportional to $-V_O$

Hence Current to Voltage Converter.

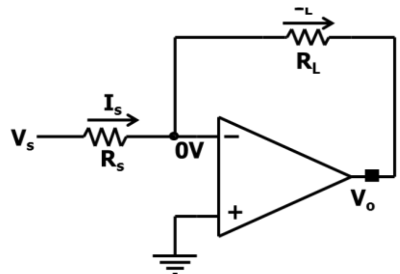


Fig 5.34 VOLTAGE TO CURRENT CONVERTER TRANS CONDUCTANCE AMPLIFIER

5.6.3 Voltage to current Converter – (Trans-conductance Amplifier) : (Refer fig 5.34)

IS = IL

$$\frac{V_S - 0}{R_S} = \quad R_L$$

$\frac{V_S}{R_S} = I_L$

$\therefore$ V_S is proportional to I_L

Hence Voltage to Current converter.

5.6.4 Op-Amp Integrator

Refer Fig 5.35. Principle : I = C $\frac{dv}{dt}$

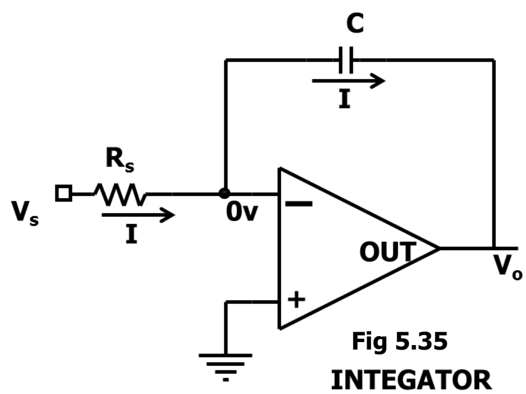


Fig 5.35
INTEGATOR

Input side	**output side**
I = $\frac{V_S-0}{R_S}$	I = C $\frac{d\,(0 - V_o)}{dt}$ = $-$ C $\frac{dV_o}{dt}$
$\frac{V_S}{R_S}$	= $-$ C $\frac{dV_o}{dt}$

Integrate on both sides

$\int_0^t \frac{V_s}{R_s} dt \quad = -C \int_0^t \frac{dV_o}{dt} dt$

$\therefore \frac{1}{R_s} \int_0^t V_s\, dt \quad = -C\, V_o$

$V_o = \frac{-1}{R_S\, C} \int_0^t V_S\ dt$ **+ initial conditions**

R_sC is known as time constant

V_{output} is the integration of the input

INPUT	OUT PUT
SIN	$-$ COS
Square wave	Triangular wave

Applications:

- In analog computers, solving differential Equations
- Signal wave shaping circuits

5.6.5 Op-Amp Differentiator: Refer 5.36

Input side

I = C $\frac{dV_S}{dt}$

C$\frac{dV_S}{dt}$

output side

I = $\frac{0-V_o}{R_f}$

= $\frac{-V_o}{R_f}$

$V_o = -R_f\, C \frac{dV_S}{dt}$

Therefore V_{output} is the differentiation of the input

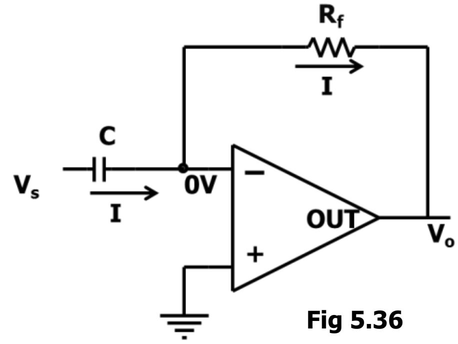


Fig 5.36
DIFFERENTIATOR

INPUT	OUT PUT
COS	- SIN
Triangular wave	Square wave

Applications:

FM demodulators

Signal wave shaping circuits

Problem 11: A sine wave of peak value 6 mv and 2 KHz frequency is applied to an op-amp integrator. R_1= 100K, C_f = 1uF. What is the output voltage?

Solution: For integrator V_o = V_o = $\frac{-1}{R_1\, C_f} \int_0^t V_{in}\, dt$ where R_1 = 100K , C_f = 1uf ,

$V_{in} = V_m \,Sin(\omega t)$, V_m = 6 mV , $\omega = 2\pi f = 2\pi\ (2000)$

Vo = $\frac{-1}{100K*1uf} \int_0^t 6mv * Sin(2\pi(2000)t)\, dt$

Vo= - 0.06 $\left[- \frac{\cos(4000\pi t)}{4\pi*1000}\right]_0^t$

Vo = 4.77(cos (4000π t) – 1) u volts

Instrumentation Amplifier

What are the Requirements of a Good Instrumentation Amplifier?

An instrumentation amplifier is used to amplify very low level low-level signals, rejecting noise and interference signals. Examples can be heartbeats, blood pressure, temperature, earth quakes and so on

Therefore, the essential characteristics of a good instrumentation amplifier are as follows.

- Inputs to the instrumentation amplifiers will have very low signal energy. Therefore the instrumentation amplifier should have high gain and should be accurate.
- The gain should be easily adjustable using a single control.
- It must have **High Input Impedance** and **Low Output Impedance** to prevent loading.
- The Instrumentation amplifier should have **High CMRR since t**he transducer output will usually contain common mode signals such as noise, when transmitted over long wires.
- It must also have a **High Slew Rate** to handle sharp rise times of events and provide maximum undistorted output voltage swing

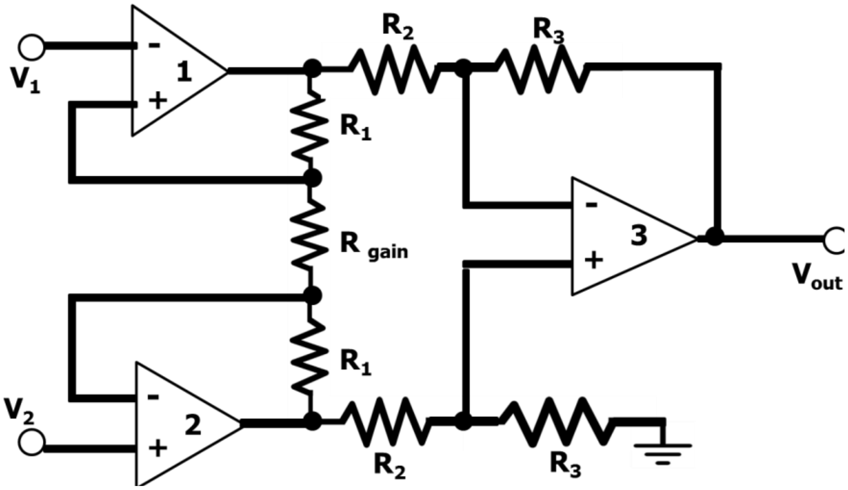


Fig 5.37 **Instrumentation amplifier**

How does it work?

The op-amps 1 & 2 are non-inverting amplifiers and op-amp 3 is a difference amplifier. These three op-amps together, form an instrumentation amplifier.

Instrumentation amplifier's final output V_{out} is the amplified difference of the input signals applied to the input terminals of op-amp 3.

Let the outputs of op-amp 1 and op-amp 2 be V_{o1} and V_{o2} respectively.

Then, $V_{out} = (R_3/R_2)(V_{o1}-V_{o2})$

Look at the input stage of the instrumentation amplifier as shown in the figure below.

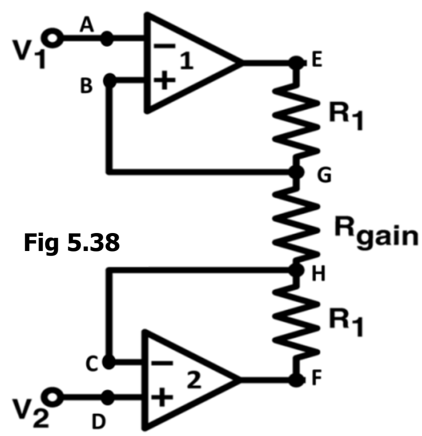


Fig 5.38

The potential at node A is the input voltage V_1. Hence the potential at node B is also V_1, from the virtual short concept. Thus, the potential at node G is also V_1.

The potential at node D is the input voltage V_2. Hence the potential at node C is also V_2, from the virtual short. Thus, the potential at node H is also V_2.

Ideally the current to the input stage op-amps is zero. Therefore the current I through the resistors R_1, R_{gain} and R_1 remains the same.

Applying Ohm's law between the nodes E and F,

$I = (V_{o1}-V_{o2})/(R_1+R_{gain}+R_1)$ ———————— 1
$I = (V_{o1}-V_{o2})/(2R_1+R_{gain})$

Since no current is flowing to the input of the op-amps 1 & 2, the current I between the nodes G and H can be given as,

$I = (V_G-V_H) / R_{gain} = (V_1-V_2) / R_{gain}$ ————————- 2

Equating equations 1 and 2,

$(V_{o1}-V_{o2})/(2R_1+R_{gain}) = (V1-V_2)/R_{gain}$
$(V_{o1}-V_{o2}) = (2R_1+R_{gain})(V_1-V_2)/R_{gain}$ ———————— 3

The output of the difference amplifier is given as,

$V_{out} = (R_3/R_2) (V_{o1}-V_{o2})$
Therefore, $(V_{o1} – V_{o2}) = (R_2/R_3)V_{out}$

Substituting $(V_{o1} – V_{o2})$ value in the equation 3, we get

$(R_2/R_3)V_{out} = (2R_1+R_{gain})(V1-V_2)/R_{gain}$
i.e. $V_{out} = (R_3/R2)\{(2R_1+R_{gain})/R_{gain}\}(V1-V_2)$

This above equation gives the output voltage of an instrumentation amplifier.

Overall gain of the amplifier is given by the term $(R_3/R2)\{(2R_1+R_{gain})/R_{gain}\}$.

The overall voltage gain of an instrumentation amplifier can be controlled by adjusting the value of resistor R_{gain}.
The common mode signal attenuation for the instrumentation amplifier is provided by the difference amplifier.

Advantages of Three Op-amp Instrumentation Amplifier:

- The gain of a three op-amp instrumentation amplifier circuit can be easily varied by adjusting the value of only one resistor R_{gain} .
- The gain of the amplifier depends only on the external resistors used.
- The input impedance is very high due to the emitter follower configurations of amplifiers 1 and 2
- The output impedance of the instrumentation amplifier is very low due to the difference amplifier 3.
- The CMRR of the op-amp 3 is very high and almost all of the common mode signal will be rejected.

Problem 12: In the circuit in fig 5.39, what is the V_0?

V1 $= - 1 \times 10^{-6}\,A \times 10\,k\Omega = - 0.1\,V$

$V_o = V1 \left(1+\frac{R_f}{R_1} \right)$

$= - 0.1 \left(1+ \frac{100K}{2K} \right) = - 5.1\,V$

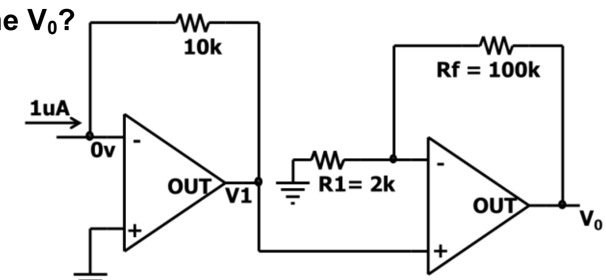


Fig 5.39

Problem 13: In the circuit in fig 5.40, If R_L varies from 1k to 60 k. What is the variation in Vo?

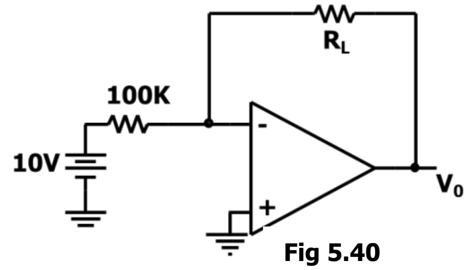


Fig 5.40

1) RL = 1K then $V_o = 10\left(-\frac{1K}{100K}\right) = -0.1$ V
2) RL = 60K then $V_o = 10\left(-\frac{60K}{100K}\right) = -6.0$ V

5.7 Differential mode and common mode signals:

Preamble: Input to an op-amp, in general, will have two types of signals called, difference signals and common mode signals.

Difference signals are those signals present at V1 and V2 which are different (not same).

Common mode signals are those signals present at V1 and V2 which are exactly same.

What is the differential gain (A_d) ?

Refer fig 5.41

V_d = V1 – V2 (V1 and V2 are different)

$V_o = A_d V_d = A_d(V1 - V2)$

Where A_d = differential gain

and V_d = differential voltage

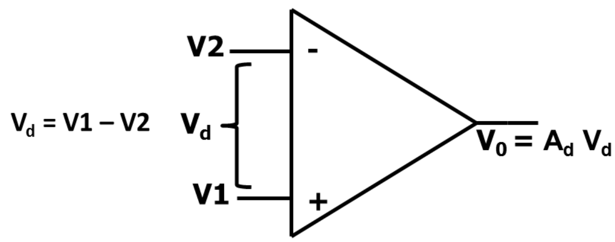


Fig 5.41 Differential Gain

What is a common mode signal ?

Refer fig 5.42. In common mode V1 and V2 are exactly same. Average level of the two input signal V1 and V2 is defined as the common mode signal

$$V_c = \frac{V1 + V2}{2}$$

For a common mode signal also, the op-amp gives an output $\mathbf{V_0 = A_c V_c}$

where A_c = common mode gain

V_c = common mode signal

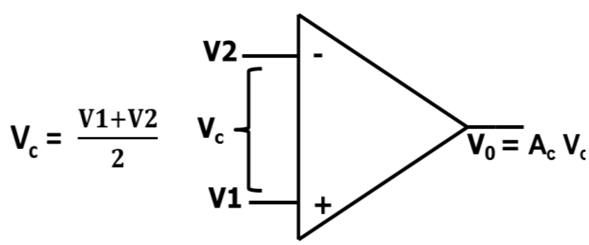


Fig 5.42 Common Mode Gain

Therefore the total output of an Op-amp

V_o = common mode output + differential mode output

$= A_cV_c + A_dV_d$

In an ideal op amp

a) Common mode gain A_c must be Zero
b) Differential mode gain A_d must be infinity

What is common mode rejection ratio (CMRR)?

CMRR is the ability of an op-amp to accept the desired differential signals and reject undesired common mode signals

CMRR = $\rho = \left|\frac{A_d}{A_c}\right|$

for ideal op amp CMRR = ∞ [since $A_d = \infty$ and $A_c = 0$]

Problem 14: In an op-amp, the non-inverting input is 500 µV and the inverting input is 200 µV. Differential gain is 3000 and CMRR = 10^5. Find the common mode gain. What is the output voltage?

CMRR = 10^5 A_d = 3000

CMRR = $\left|\frac{A_d}{A_c}\right| = \left|\frac{3000}{A_c}\right|$

Therefore A_c = 0.03

V_d = 500 - 200 = 300 µV.

$V_c = \frac{500+200}{3}$ = 350 µV

$V_o = A_cV_c + A_dV_d$

= 3000 X 300 µV + 0.03 X 350 µV

= 900.1015 mV

5.8 Ideal Operational amplifier.

What are the characteristics of an op amp?

1. **Infinite open loop voltage gain (A_V):** The ideal OP-amp has a gain of infinity. (However, in practice, A_V will be around 10000)
2. **Infinite bandwidth:** The bandwidth of an op-amp is infinite. It has no low frequency cut –neither off, nor high frequency cut –off.
3. **Infinite input impedance (R_{in}):** $R_{in} = \infty$. This means, the op amp does not require any input current and in fact the op-amp does not draw any input current.
4. **Infinite output impedance (R_{out}):** R_{out} = 0. This means, the op-amp output will remain at the same level whether the load $R_L = \infty$ or R_L = 0. The drive capability of the op-amp is infinite
5. Z**ero offset voltage (V_{IOS}):** If the inputs, V1 = V2 = 0 V, the output will be exactly 0 V.
6. **Infinite Common Mode Rejection Ratio – CMRR (ρ):**
7. CMRR = ∞. If the inputs are equal and identical (V1 =V2), the output will be zero volts. This will ensure, noise signals at the input, will be rejected by the op-amp.
8. **Infinite slew rate (S= ∞) :** If the input is a step voltage, the output also will be a step output. Slew rate is an indication of the rate at which the op-amp output rises. Slew rate S = $\frac{dV_o}{dt}$.
9. **Power supply rejection ratio (PSRR) : Op amp has a good PSRR. Therefore even i**f the power supply voltage fluctuates, the output will still be steady (will not fluctuate)
10. **Temperature stability:** The op amp characteristics will not change due to temperature variations .

Draw a block diagram of an op-amp and explain its operation.

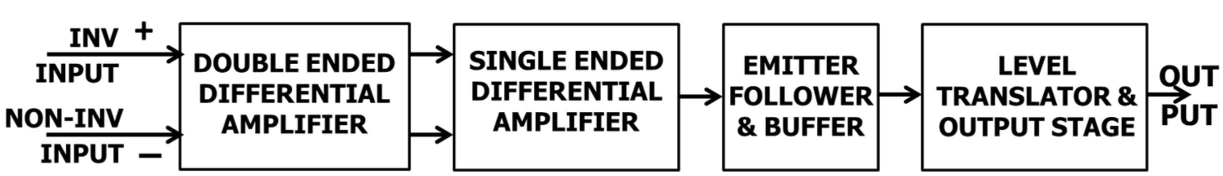


Fig 5.43 Operational Amplifier Basic Block Diagram

Op amp has 4 stages. Op amp can amplify both ac signals and DC signals

1) Input stage :
a) It is a double ended differential amplifier.
b) Two inputs & two outputs. It is a DC amplifier
c) This stage provides maximum gain for the op-amp.
d) Has high input impedance and low output impedance.

2) Single ended differential amplifier :
a) Provides moderate gain. This is also a DC amplifier
b) Two inputs and single output.

3) Emitter follower
a) It is a buffer.
b) Unity gain. DC amplifier, again.

4) Level translator and output stage :
a) All the previous 3 Stages are DC amplifiers. There will be a gradual DC shift in these 3 amplifiers and this DC build up needs to be reset, to ground potential. This stage does this function of level shifting .
b) The o/p stage presents, a low output impedance to the load
c) It can provide large voltage swings, in the output
d) It can source or sink large load currents.

5.9 Schmitt Trigger using Op-amps

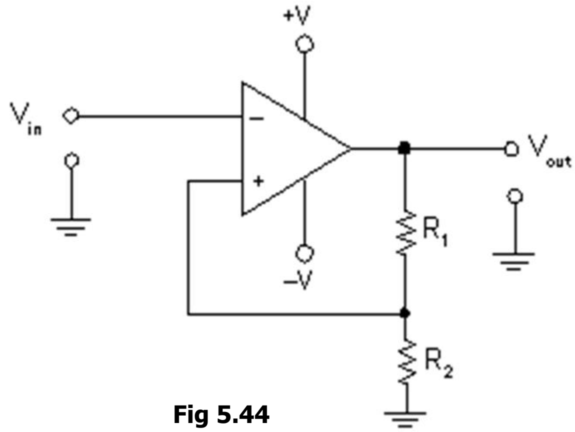
What are the circuits used to generate square wave?
Ans: Schmitt Trigger, Astable Multivibrator, Zero Cross Detector, PLL.

What is a Schmitt Trigger?

- Schmitt trigger is a regenerative comparator.
- Employs positive feedback
- It converts sinusoidal input into a square wave output.
- The output of Schmitt trigger swings at upper and lower threshold voltages, which are the reference voltages of the input waveform.
- It is a bi-stable circuit in which the output swings between two steady-state voltage levels (High and Low) when the input reaches certain designed threshold voltage levels.

What are UTP and LTP?
UTP: Upper Trigger Point.
LTP: Lower Trigger Point.

What is hysteresis?
See figure on the right side.. When the input is higher than a certain chosen threshold (UTP), the output is low.
.



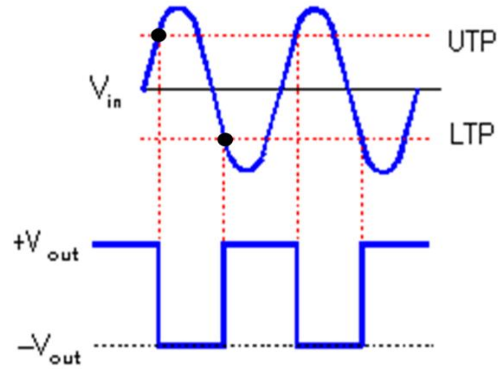


Fig 5.44

UTP: Upper Trigger Point. **LTP: Lower Trigger Point.**

When the input is below a threshold (LTP), the output is high; when the input is between the two, the output retains its current value. This dual threshold action is called hysteresis.
V Hysteresis = UTP-LTP in our example

Define UTP and LTP. What are the values of UTP and LTP for the above circuit?
Upper threshold (Trigger) point, Lower Threshold (Trigger) points – these are the points where the input signal is compared. The values are UTP = $+V * R_2 / (R_1 + R_2)$ and LTP = $-V^* R_2 / (R_1 + R_2)$
For what requirements, Schmitt Trigger is used?
When two levels are to be compared there may be oscillation (or hunting) at the border. Having hysteresis prevents this oscillation problem is solved.
What is the basic difference between the comparator and Schmitt trigger?
Comparator compares always with a fixed reference voltage (single reference) whereas Schmitt trigger compares with two different voltages called UTP and LTP.

For the Schmit trigger circuit below, what are the UTP, LTP values?

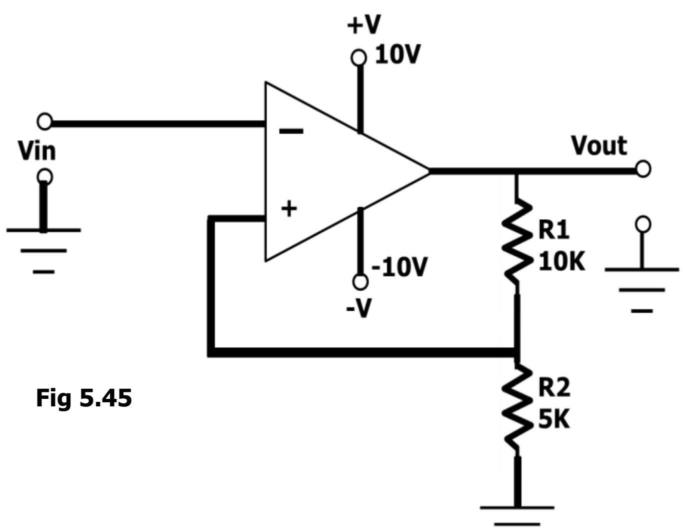


Fig 5.45

We know that UTP = +V * R_2 / (R_1 + R_2) and LTP = -V* R_2 / (R_1 + R_2)

UTP = +10V * $\frac{5K}{5K+10K}$ = + 3.33 V

LTP = -10V * $\frac{5K}{5K+10K}$ = - 3.33 V

5.10 Filters using Operational Amplifiers

5.10.1 What is a filter?

A filter is a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band.

What are the classifications?

Based on their frequency response: Low pass, high pass, bandpass and band stop (notch) filters

Based on devices used: Active or passive filters

- Passive filters employ only passive components such as resistors, capacitors and inductors.
- Active filters employ active components such as operational amplifiers, transistors or FET's within their circuit design.
- Passive Filters cannot provide gain whereas active filters provide gain.
- Load characteristics are far better in active filters since they use op-amps or emitter follower transistors.

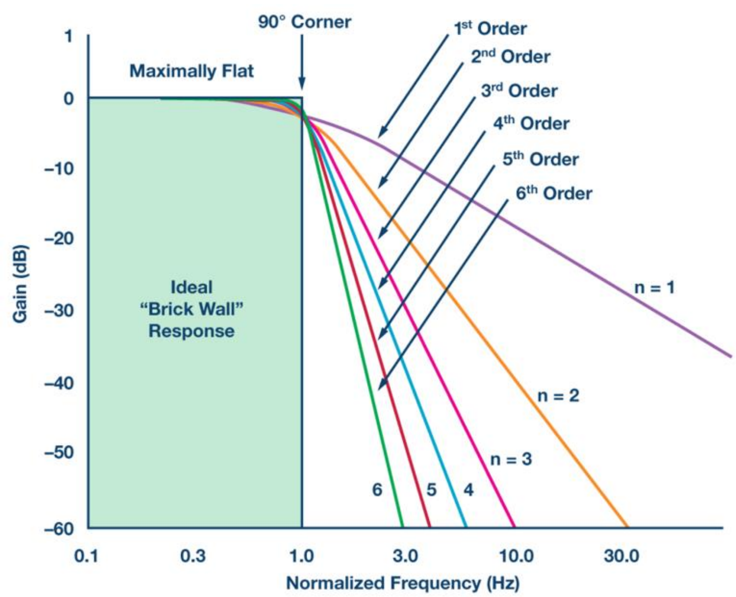


Fig 5.46

The most common active filters are **Butterworth, Chebyshev and Bessel and elliptic filters.**

- **Butterworth filter** has a flat response that rolls-off at 40dB per decade. The initial roll off rate is quite gradual. The Butterworth filter is also termed a maximally flat magnitude filter.
- **Chebyshev filter** has a much sharper initial roll-off, but at the roll off point the response exhibits kinks.
- **Bessel filter** has a performance similar to a Butterworth, but with a slower initial roll-off.
- **Elliptic filter** has the sharpest roll-off of all filters in the transition region but has ripples in both the pass band and stop band regions.

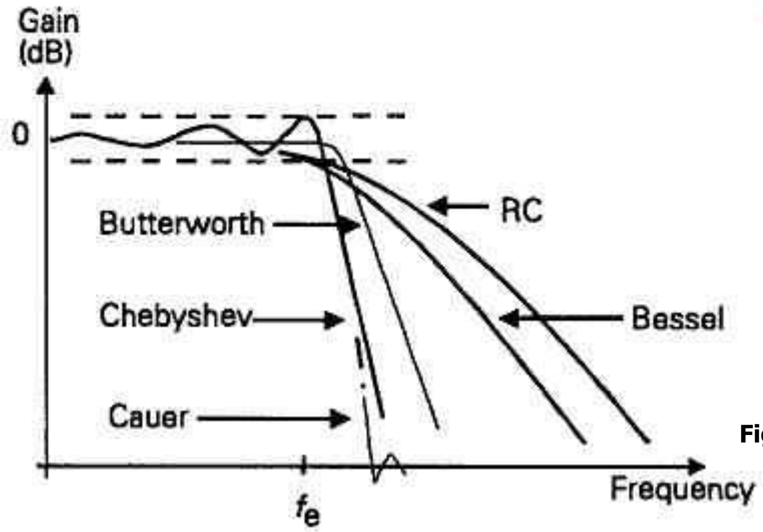


Fig 5.47

Ideal Filter Responses:

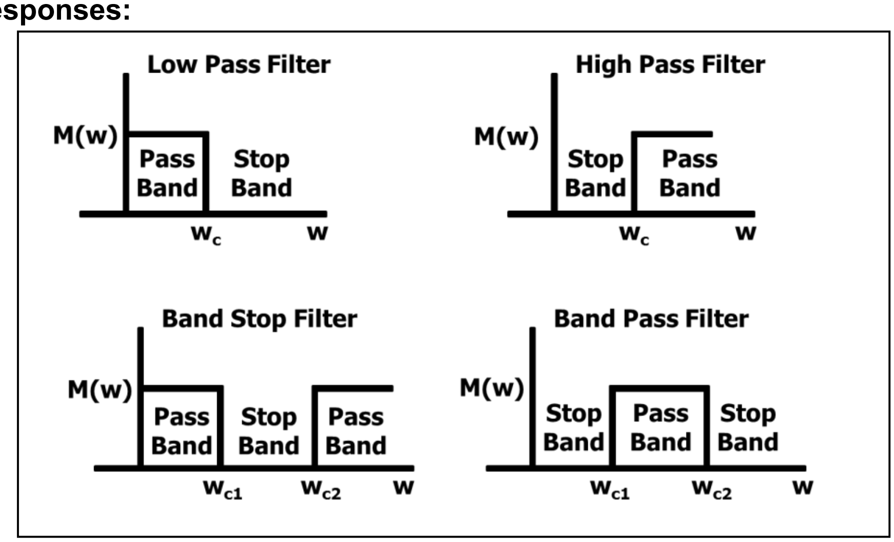


Fig 5.48

5.10.2 Low pass Filter Analysis

A first order low pass filter is shown in the figure.

What is this circuit? A simple integrator. Note that integrator is the basic building block for low pass filters

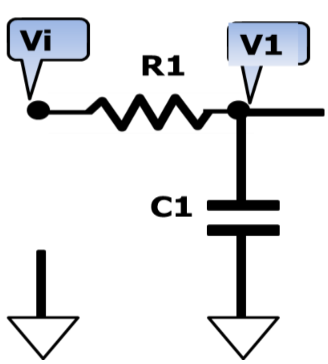


Fig 5.49

First order low pass analysis

Assume $Z_1 = \frac{1}{j\omega C_1}$,

$$V_1 = V_i \frac{Z_1}{R_1+Z_1} = V_i \frac{\frac{1}{j\omega C_1}}{R_1+\frac{1}{j\omega C_1}} = V_i \frac{1}{j\omega C_1 R_1+1} = V_i \frac{1}{sC_1R_1+1} \quad (s = j\omega)$$

Transfer function is

$$\frac{V_1}{V_i} = \frac{1}{sC_1R_1+1}$$

Output reduces (attenuates) inversely as the frequency. If frequency doubles output is half. (- 6 dB for every doubling of frequency or – 6 dB per octave).

This is a low pass filter of first order and the roll of is at -6 dB per octave.

5.10.3 Second order low pass filter

A second order low pass filter is shown in the figure.

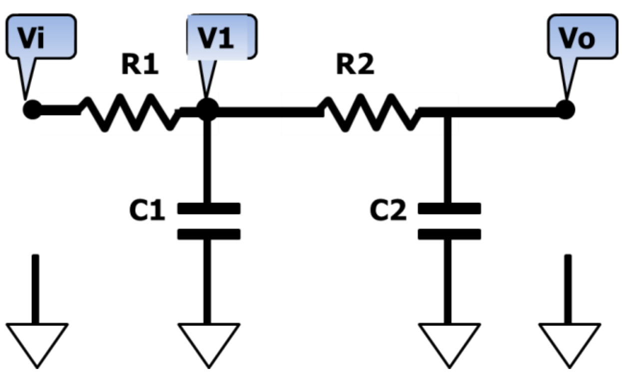


Fig 5.50

Second order low pass analysis

Assume $Z_1 = \frac{1}{j\omega C_1}$,

$$V_1 = V_i \frac{Z_1}{R_1+Z_1} = V_i \frac{\frac{1}{j\omega C_1}}{R_1+\frac{1}{j\omega C_1}} = V_i \frac{1}{j\omega C_1 R_1+1} = V_i \frac{1}{sC_1R_1+1} \quad (s = j\omega)$$

Next,

Assume $Z_2 = \frac{1}{j\omega C_2}$,

$$V_o = V_1 \frac{Z_2}{R_2+Z_2} = V_1 \frac{\frac{1}{j\omega C_2}}{R_2+\frac{1}{j\omega C_2}} = V_1 \frac{1}{j\omega C_2 R_2+1} = V_1 \frac{1}{sC_2R_2+1} \quad (s = j\omega)$$

$$= V_i \frac{1}{sC_1R_1+1}\frac{1}{sC_2R_2+1}$$

$$= \frac{1}{s^2R_1R_2C_1C_2+s(R_1C_1+R_2C_2)+1}$$

Therefore transfer function is a second order equation.

$$\frac{V_o}{V_i} = \frac{1}{s^2R_1R_2C_1C_2+s(R_1C_1+R_2C_2)+1}$$

Output reduces (attenuates) inversely as the square of the frequency. If frequency doubles output is $1/4^{th}$. (- 12 dB for every doubling of frequency or – 12 dB per octave).

This is a low pass filter of second order and the roll of is at -12 dB per octave.

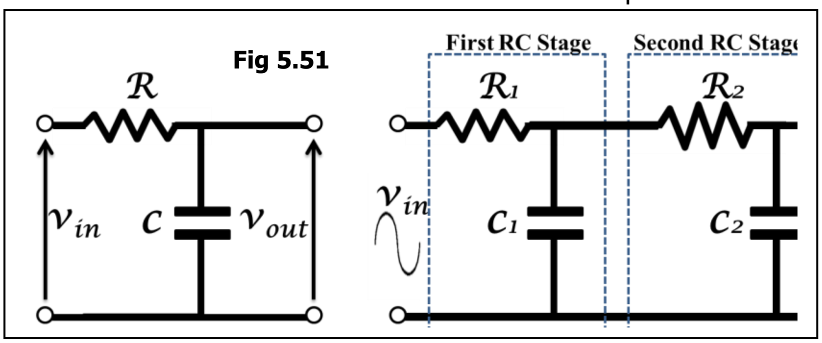


Fig 5.51

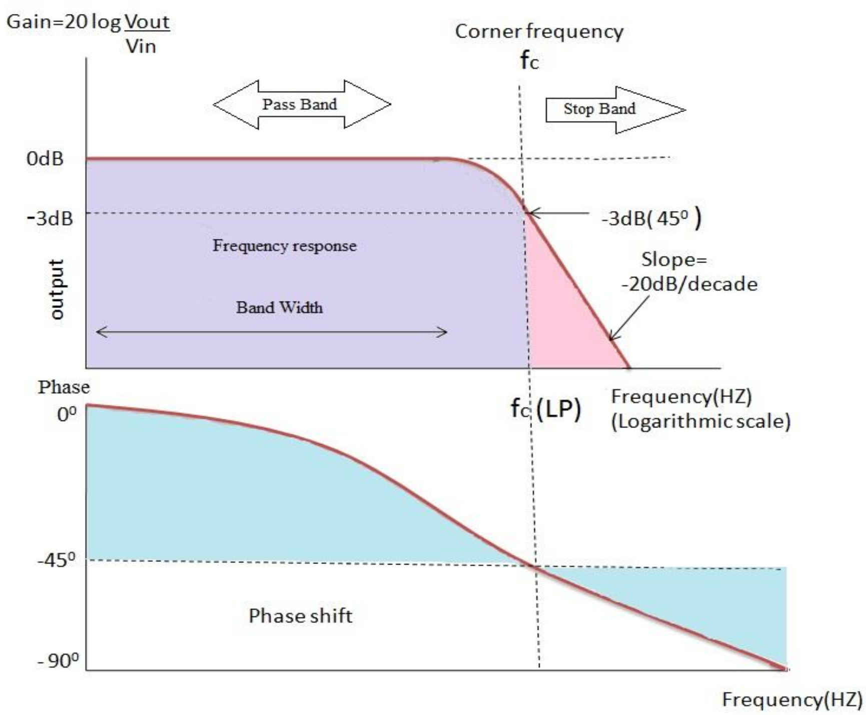


Fig 5.52

5.10.4 High pass filter examples

Note that Differentiator is the basic building block for high pass filters

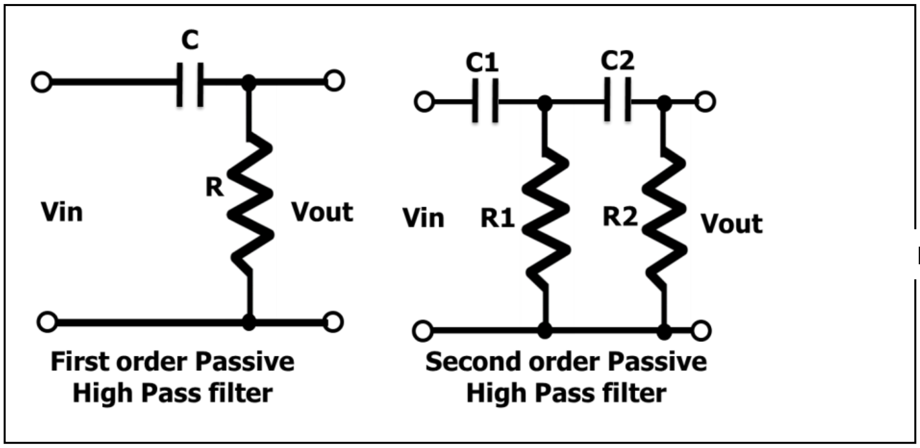


Fig 5.53

OP-AMP AS INTEGRATOR AND DIFFERENTIATOR

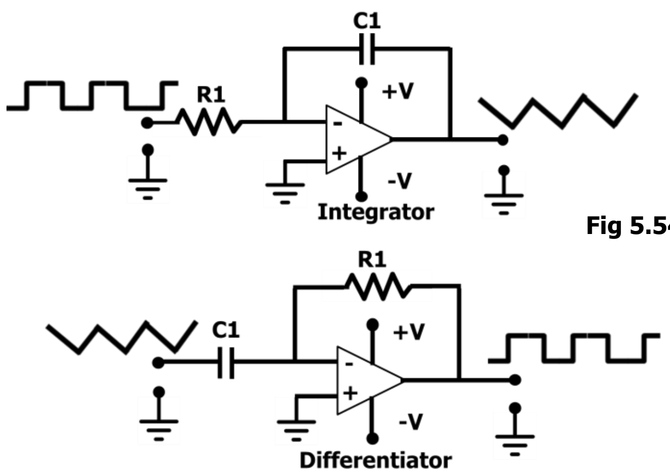


Fig 5.54

5.10.5 SECOND ORDER ACTIVE LOW PASS FILTER

Aim: To obtain the frequency response of an active low pass Butterworth filter for the desired Cut off frequency

Given Specification: Design the low pass filter with cut off frequency fc=1 kHz

<u>Basic circuit diagram</u>

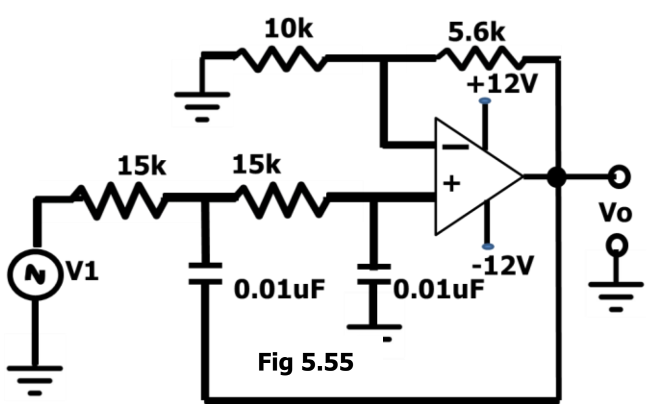


Fig 5.55

The normalised frequency response of the second order low pass filter is fixed by the RC network and is generally identical to that of the first order type. The main difference between a 1st and 2nd order low pass filter is that the stop band roll-off will be twice the 1st order filters at 40dB/decade (12dB/octave) as the operating frequency increases above the cut-off frequency fc.

Design:
For a 2nd order Filter, Cut off frequency f_c = 1 / 2πRC Hz
Let us design a low pass filter with f_c = 1 kHz and R = 15 kΩ

Therefore, $1*10^3 = \frac{1}{2\,\pi * 15 * 10^3 * C}$

Therefore, C = 0.01 μF

The pass band gain of the filter, AF = $(1 + \frac{R_f}{R_1})$

How to design the Gain of the amplifier (Butterworth):

- In active second order filters, there is a parameter called damping factor, ζ (zeta). There is a parameter called quality factor Q. These two are inversely proportional.
- Both Q and ζ are independently determined by the gain of the amplifier A. If Q decreases the damping factor increases.
- Look at the frequency response curve esp. around the cut-off region. Low pass filters have a peaking tendency (overshoot) around the cut-off frequency as seen in the figure. This is called a resonant peak. In this cut-off region, the gain can increases rapidly due to resonance effects of the amplifiers gain.
- Q, the quality factor, represents the "peakiness" of this resonance peak. Peakiness is, the height and narrowness around the cut-off frequency point, f_C. A filter's gain can control this peakiness.

Generally to maintain stability, an active filter's gain must not be more than 3 and is best expressed as:

The Quality Factor, "Q"   A= 3 – (2 X ζ)

Where $\zeta = \frac{3-A}{2} = \frac{1}{2Q}$

$\therefore A = 3 - \frac{1}{Q}$

Second Order Filter Amplitude Response (Butterworth)

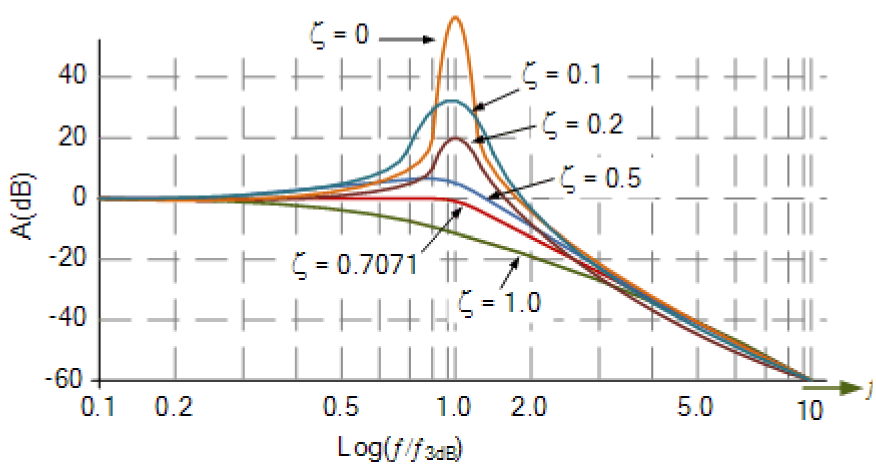


Fig 5.56

The amplitude response of the second order low pass filter varies for different values of damping factor, ζ.

- When ζ = 1.0 or more (2 is the maximum) the filter becomes what is called "overdamped" with the frequency response showing a long flat curve.
- When ζ = 0, the filters output peaks sharply at the cut-off point resembling a sharp point at which the filter is said to be "underdamped".

Then somewhere in between, ζ = 0 and ζ = 2.0, there must be a point where the frequency response is of the correct value, and there is. This is when the filter is "critically damped" and occurs when ζ = 0.7071.

With ζ = 0.7071, the gain of a second order Butterworth filter, AF = 1.586,

Let R1 = 10KΩ . Therefore, Rf = 5.86kΩ

(Note that AF = 1.586 IS VALID ONLY FOR BUTTERWORTH RESPONSE DESIGNS. For a Bessel second order filter design: 1.268, and for a Chebyshev low pass design: 1.234.)

According to the design,

R1=10kΩ , Rf = 5.6kΩ , R =15kΩ , C=0.01uF

A typical frequency response waveform is as follows

We can see that 3dB down frequency occurs at f = 1.0 kHz. So, Cut-off frequency f_c=1 kHz.

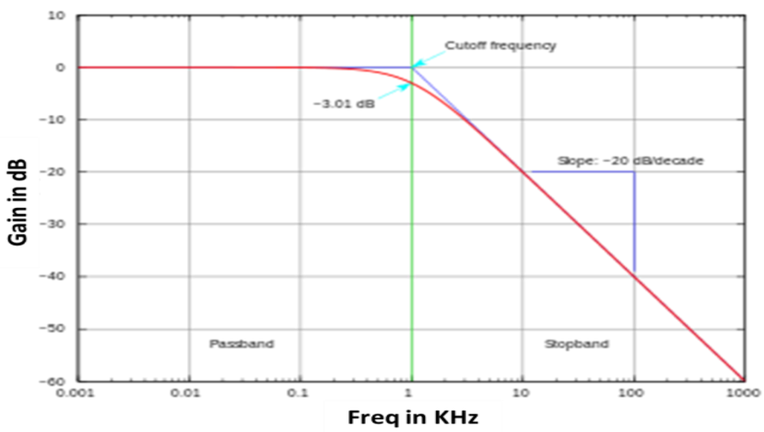


Fig 5.57

5.10.6 SECOND ORDER ACTIVE HIGHPASS FILTER

Aim: To obtain the frequency response of an active high pass Butterworth filter for the desired Cut off frequency.

Given Specification: Design the high pass filter with cut off frequency fc = 2 kHz

Basic circuit diagram

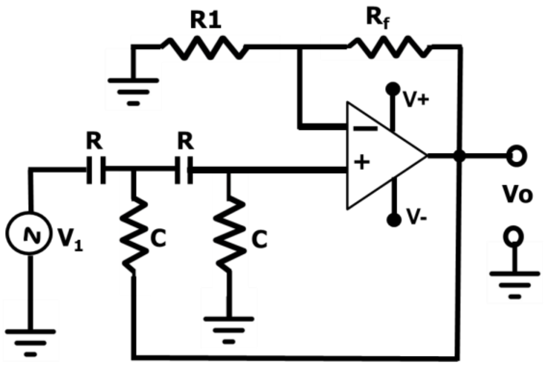


Fig 5.58

Design:

For a 2nd order Filter, fc = 1 / 2πRC Hz

Let fc = 2 kHz and R = 10 kΩ

Therefore, $2*10^3 = \frac{1}{2\pi * 10 * 10^3 * C}$

Therefore, C = 0.8000 pF

The pass band gain of the filter, AF = (1+R f / R1)

From the transfer function for a second order Butterworth filter, AF = 1.586, Let R1 = 10KΩ

Rf = 5.86kΩ

The pass band gain of the filter, AF = $(1 + \frac{R_f}{R_1})$

According to the design,

R1=10kΩ , Rf=5.86kΩ , R =10kΩ , C=8000pF

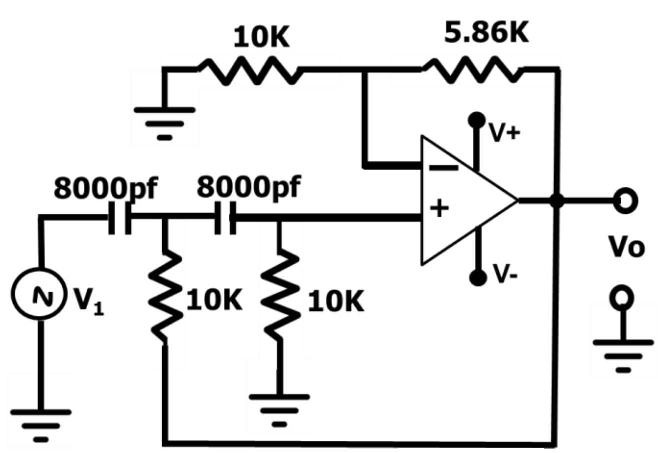


Fig 5.59

5.10.7 Design of a SECOND ORDER ACTIVE BAND PASS FILTER

Aim: To obtain the frequency response of an active band pass filter from 2 KHz to 10 KHz passband and to verify the roll off.

<u>Design a 2nd order High pass filter 2 KHz cutoff.</u>
Filter, F= 1 / 2πRC Hz

For High pass section
Let FL = 2 KHz and R = 33 K

Design:
For a 2nd order Filter, F= 1 / 2πRC Hz

(i) For High pass section
Let FL = 2 KHz and R = 33 K
Therefore, $2*10^3 = \frac{1}{2\pi * 33 * 10^3 * C}$
Therefore, C = 2700 pF (approx)

(i) For Low pass section
Let FL = 10 KHz and R = 33 K
Therefore, $10*10^3 = \frac{1}{2\pi * 33 * 10^3 * C}$
Therefore, C = 540 pF (approx)

Pass band gain of the filter,
AF = (1+R f / R1)
For a second order filter, AF = 1.586, Let R1 = 10K
RF = 5.86 k
The Center frequency FC =$\sqrt{FH * FL}$
Hence f_C = 4.5 KHz (approx)

Circuit Diagram:-

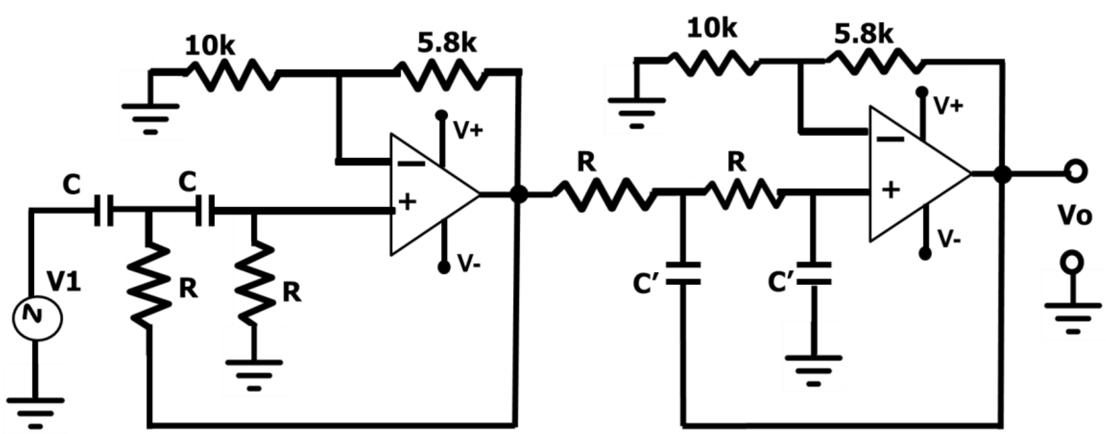


Fig 5.60 BAND PASS FILTER

5.10.8 SECOND ORDER ACTIVE BAND REJECT (BANDSTOP) FILTER

Design of a SECOND ORDER ACTIVE BAND STOP (BAND ELIMINATION, BAND REJECT) FILTER

Aim: To obtain the frequency response of an active band stop filter from 2 KHz to 10 KHz stop band and to verify the roll off.

<u>Design a 2nd order High pass filter 10 KHz cutoff.</u>

Filter, F= 1 / 2πRC Hz

For High pass section

Let FL = 10 KHz and C = 0.01uF

Design:

For a 2nd order Filter, F= 1 / 2πRC Hz

(i) For High pass section

Let FL = 10 KHz and C = 0.01uF

Therefore, $10*10^3 = \frac{1}{2\,\pi * 0.01 * 10^{-6} * R}$

Therefore, R = 1.59 K ohms

(i) For Low pass section

Let FL = 2 KHz and R = 33 K

Therefore, $2*10^3 = \frac{1}{2\,\pi * 33 * 10^3 * C}$ $\qquad$ $1 / 2*\pi*33*10^3 *C$

Therefore, C = 2700 pF (approx)

Circuit Diagram:-

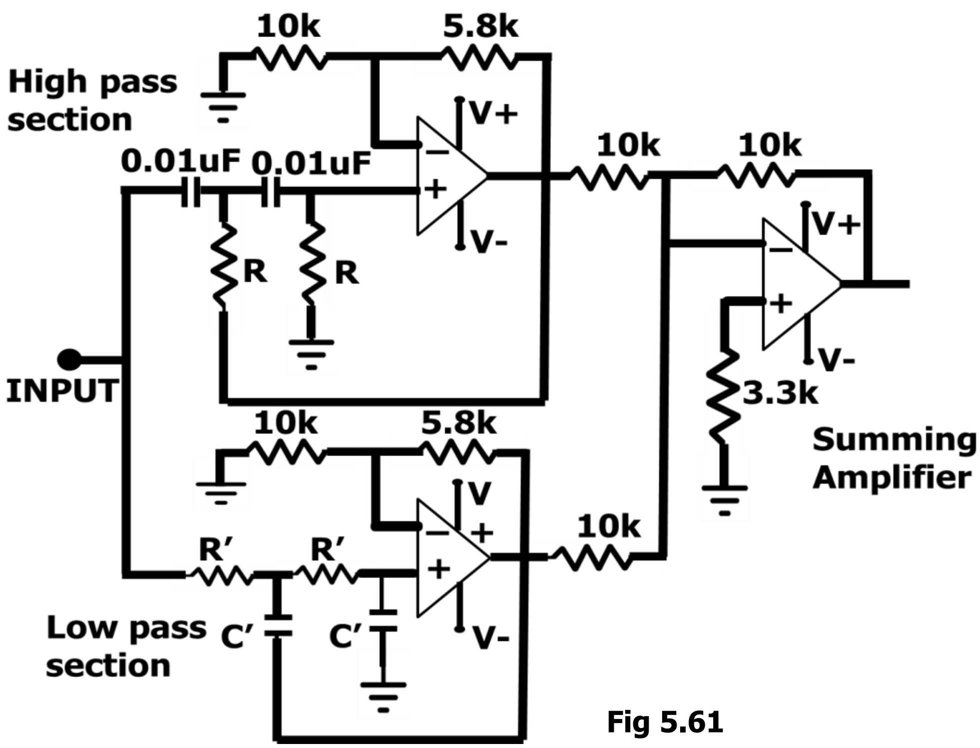


Fig 5.61

Pass band gain of the filter,

$AF = (1+R_f / R_1)$

For a second order filter, AF = 1.586, Let R_1 = 10K

R_f = 5.86 k

The Center frequency FC $=\sqrt{\mathrm{FH} * \mathrm{FL}}$

Hence f_C = 4.5 KHz

Chapter 6 OSCILLATORS

6.1 FEEDBACK CONCEPTS ●

We had seen feedback briefly in op-amp circuits. Feedback in general refers to a portion of the signal from output being handed over back to input deliberately or inadvertently.

There are two types: positive feedback and Negative feedback.

Negative feedback: If the signal fed back opposes the input signal (opposite phase) it is negative feedback. This reduces the overall gain of the circuit.

Positve feedback: If the signal fed back aids the input signal (same phase) it is positive feedback. This increases the overall gain of the circuit and leads to oscillations.

Advantages of negative feedback:

- 1. Higher input impedance.
- 2. Better stabilized voltage gain.
- 3. Improved frequency response (fidelity)
- 4. Lower output impedance.
- 5. Reduced noise.
- 6. More linear operation.
  - It reduces all kinds of distortions (amplitude, frequency, phase and harmonic)

Disadvantages of negative feedback:

Negative feedback results in decreased gain.

Advantages of positive feedback:

Increases the gain of the system.

If controlled well, helps build oscillators , a very vital element in Electronic design systems.

Disadvantages of positive feedback:

If handled badly, can result in uncontrolled oscillations, effectively jamming the intended application.

Positive feedback drives a circuit into oscillation as in various types of oscillator circuits.

A typical feedback connection is shown in Fig below.

The input signal V_s is applied to a mixer network, where it is combined with a feedback signal V_f .

The difference of these signals V_i is then given as the input voltage to the amplifier.

A portion of the amplifier output V_o is connected to the feedback network (β), which provides a reduced portion of the output as feedback signal (V_f) to the input mixer network.

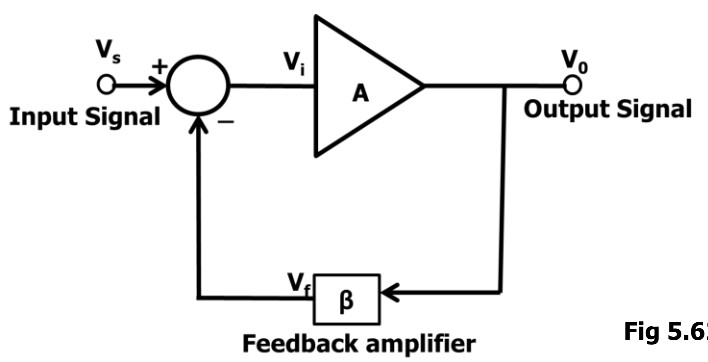


Fig 5.62

Simple block diagram of a feedback amplifier.

Gain with Feedback
What is the gain of such a feedback system?

If there is no feedback (Vf = 0), the voltage gain of the amplifier stage is

A = $\frac{V_O}{V_S} = \frac{V_O}{V_i}$

If a feedback signal V_f is fed back to the input, then $V_i = V_s - V_f$

But Vo $= AV_i = A(V_s - V_f)$

$= AV_s - AV_f$

$= AV_s - A\beta V_o$

$\therefore V_o(1+A\beta) = AV_s$

$\therefore$ The overall voltage gain with feed back is $A_f = \frac{V_O}{V_S} = \frac{A}{(1+A\beta)}$

6.2 Types of FEEDBACK configurations

There are four basic feedback configurations.

1. Voltage-series feedback
2. Voltage-shunt feedback
3. Current-series feedback
4. Current-shunt feedback

Figure 5.63 shows all four types.
Voltage feedback type, feeds some portion of the the output voltage back as input.
Current feedback type, feeds some portion of the output current back as input.

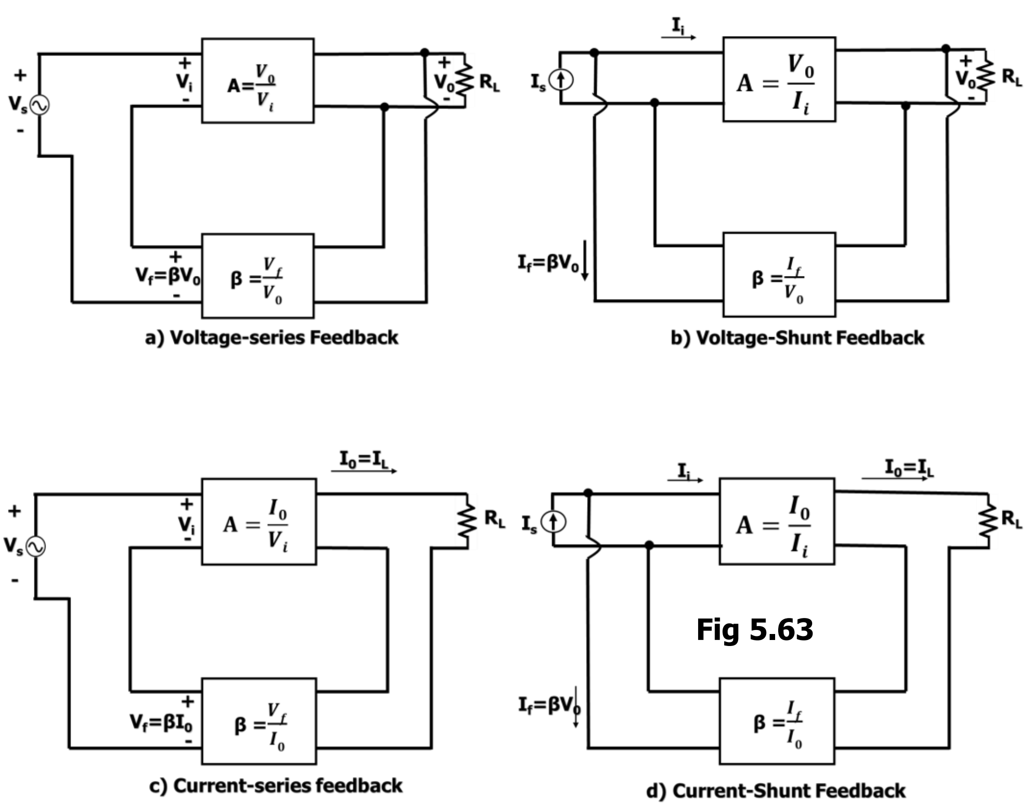


Fig 5.63

If the feedback signal is in series with the input signal then it is called series feedback.
If the feedback signal is in parallel (shunt) with the input signal then it is called parallel (shunt) feedback

Feedback amplifier types: (a) voltage-series feedback, (b) voltage-shunt feedback.
(c) current-series feedback. (d) current-shunt feedback.

Series feedback increases the input resistance and shunt feedback decreases the input resistance.

Voltage feedback decreases the output impedance and current feedback increases the output impedance.

It is desirable to have higher input impedance and lower output impedance in circuits. Therefore voltage-series feedback connections are always preferred.

6.3 Gain with Feedback

In this section we examine the gain of each of the feedback circuit connections of Fig.5.63 Amplifier alone has a gain of A. The feedback factor is that of the amplifier stage. With feedback β.The overall gain of the circuit is reduced by a factor (1 + A β).

		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without Feedback	A	$\frac{V0}{Vi}$	$\frac{V0}{Ii}$	$\frac{I0}{Vi}$	$\frac{I0}{Ii}$
Feedback	β	$\frac{Vf}{V0}$	$\frac{If}{V0}$	$\frac{Vf}{I0}$	$\frac{If}{I0}$
Gain with Feedback	A_f	$\frac{V0}{Vs}$	$\frac{V0}{Is}$	$\frac{I0}{Vs}$	$\frac{I0}{Is}$

The table gives a summary of the gain (A), feedback factor (β), and gain with feedback (A_f).

Voltage-Series Feedback:

If there is no feedback($V_f=0$), the voltage gain of amplifier of 1st stage is

$A = \frac{V_0}{V_s} = \frac{V_0}{V_i}$

A feedback signal V_f is connected in series with the input, then

$V_i = V_s - V_f$

Since $V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$

then$(1 + \beta A)V_o = AV_s$

So that the overall voltage gain with feedback is

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

Equation shows the gain with feedback is the amplifier gain reduced by the factor (1+Aβ). This factor will be seen also to effect input and output impedance among other circuit features

Voltage Shunt Feedback:

$$A_f = \frac{V_o}{I_s} = \frac{A\,I_i}{I_i + I_f} = \frac{A\,I_i}{Ii + \beta V0} = \frac{A\,I_i}{I_i + \beta A\,I_i}$$

$$A_f = \frac{A}{1 + A\beta}$$

Input Impedance with Feedback:

Voltage Series Feedback:

Refer Fig 5.63. The input impedance can be determined as follows:

$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i} = \frac{V_s - \beta A\,V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A\,V_i$$

$$V_s = I_i Z_i + \beta A\,V_i = I_i Z_i + \beta A I_i Z_i$$

$$Z_{if} = \frac{V_s}{I_i} = Z_i + A\beta Z_i = Z_i(1 + A\beta)$$

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor (1+Aβ), and applied to both voltage-series and current-series configurations.

6.4 Barkhausen Criteria for oscillations

- Positive feedback increases the loop gain to greater than unity (**A_f >1**).
- Ensure that the phase of the signal fed back is same as that present at the input **(360 degrees)**.
- These two conditions will ensure that the amplifier produces a continuous time varying signal.
- At this time, if the input signal totally removed (keeping the feedback signal in-tact), the amplifier will continue to produce the same continuous time varying signal.
- In other words the system oscillates. Such circuits are known to be oscillators.

Look at the figure 5.64 below.

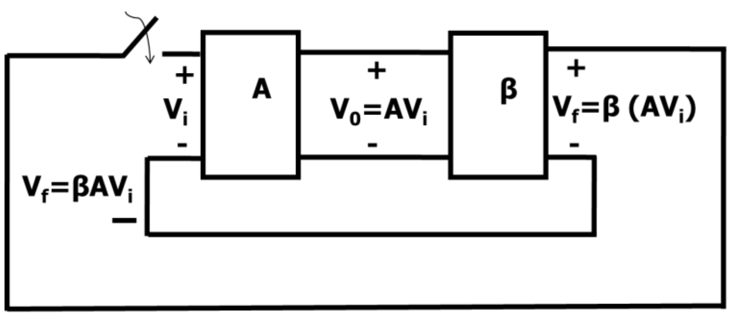


Fig 5.64

Feedback circuit used as an oscillator

1. When the switch at the input is open, no oscillations happen.
2. Imagine there is an imaginary voltage at the amplifier input V_i (maybe a noise signal).
3. This produces some output V_o = AV_i as amplifier output.

4. This in turn, produces a feedback voltage output $V_f = \beta AV_i$
5. **βA** product is known as **loop gain.**
6. If the basic amplifier and the feedback network ensure that the feedback voltage is of correct magnitude (.1) and correct phase 360°, V_f can be made equal to V_i

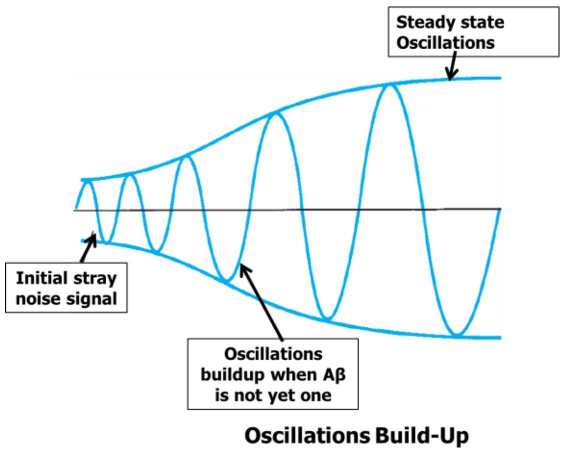


Fig 5.65

7. Now close the switch and remove the imaginary voltage. The circuit will **run by itself** since the feedback input is of correct phase and right magnitude.

1) All these will happen if and only if βA > 1
2) All these will happen if and only if the feedback is positive (same phase or 360°)

Conditions 1 and 2 above are known as Barkheusen criteria

6.5 RC PHASE SHIFT OSCILLATOR.

The RC Oscillator Circuit
RC Oscillators use a 3 stage an RC network and an amplifier and to produce oscillations due to the phase shift between the stages. Barkheusen criteria is the main focus.

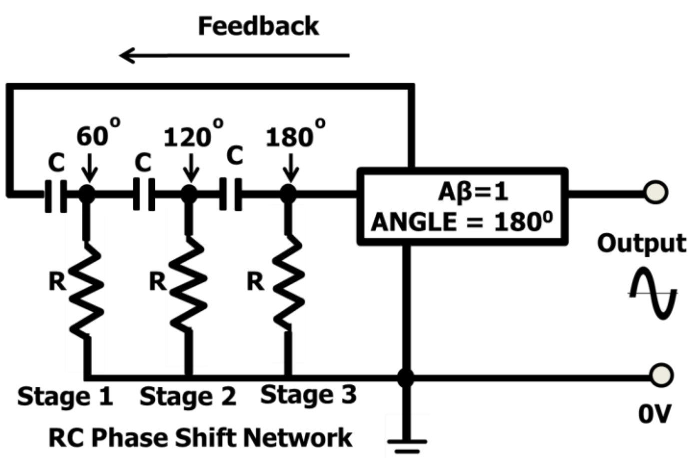


Fig 5.66

Each RC combination is designed to give a 60° shift, With 3 such RC combinations a phase shift of 180° is achieved. The figure illustrates this.

Refer figure 5.66. **RC Oscillator** consists of a 3 stage RC network which produces a phase shift of 180^o and an inverting amplifier which produces another 180^o. Therefore the total phase shift is 360^o, one of the conditions for oscillations..

RC Phase Shift Oscillator details:

- The energy storage capacity of a capacitor in this circuit produces a noise voltage which is like to a small sine wave, it is then amplified using an inverting amplifier.
- The 3 stage RC phase shift network attenuates the signal by a factor of 1/29. Therefore the gain of the inverting amplifier should be at least 29 in order to keep the loop gain as unity.
- RC Oscillators are constant and provide a well-shaped sine wave output with the frequency being proportional to 1/RC.

Frequency of oscillation (F)

F = 1/2πRC√2N

= 1/2πRC√2×3 (since N = Number of stages =3)

= 1/2πRC√6

Gain of the Op Amp inverting amplifier (G)

Gain = 29

The feedback RC network offers an attenuation that is 1/29, so the gain of the inverting amplifier should be 29

By cascading four RC stages together (4 x 45^o), the stability of the oscillator can be greatly improved.

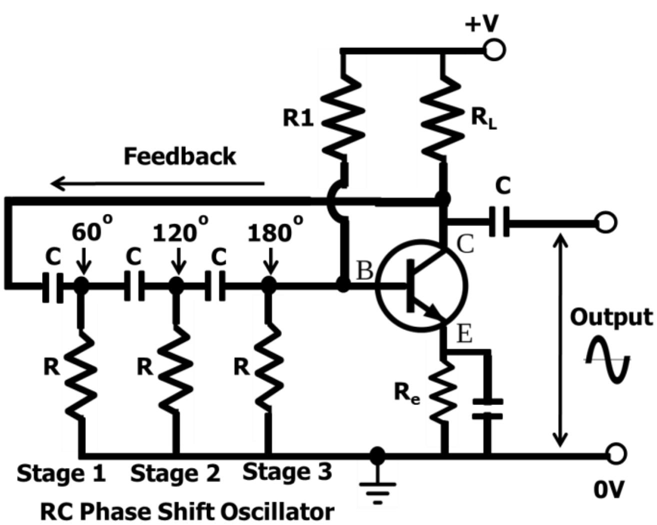


Fig 5.67

Design example:

To design and test a RC-phase shift oscillator for a frequency of 10 kHz.

DESIGN OF TANK CIRCUIT:

$\mathbf{f_O} = \dfrac{\mathbf{1}}{\mathbf{2\pi\, RC\sqrt{6}}}$ Given f_O = 10KHz

Assume **C = 0.02** μ**F**

R = 1/(2π x 0.02 x 10^{-6} x 10 x 10^3 x $\sqrt{6}$) **= 330** ohms

6.6 Op-amp RC Oscillator Circuit

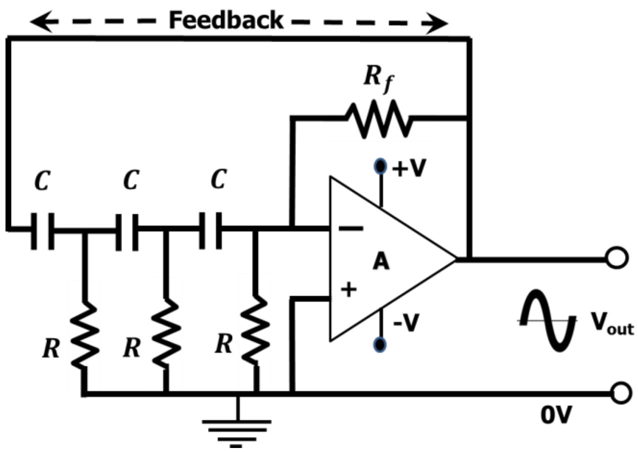


Fig 5.68

As the feedback is connected to the inverting input, the operational amplifier is therefore connected in its “inverting amplifier” configuration which produces the required 180^o phase shift while the RC network produces the other 180^o phase shift at the required frequency (180^o + 180^o).

6.7 The Wien Bridge Oscillator

The Wien Bridge Oscillator uses two RC networks connected together to produce a sinusoidal oscillator. Recall, RC phase shift Oscillator employed 3 RC combinations with an inverting amplifier.

The **Wien Bridge Oscillator** uses a feedback circuit consisting of a series RC circuit (High pass Filter) connected with a parallel RC (Low pass Filter) of the same component. At the resonant frequency f_o the phase shift is 0^o or 360^o. Refer figure below.

RC Phase Shift Network

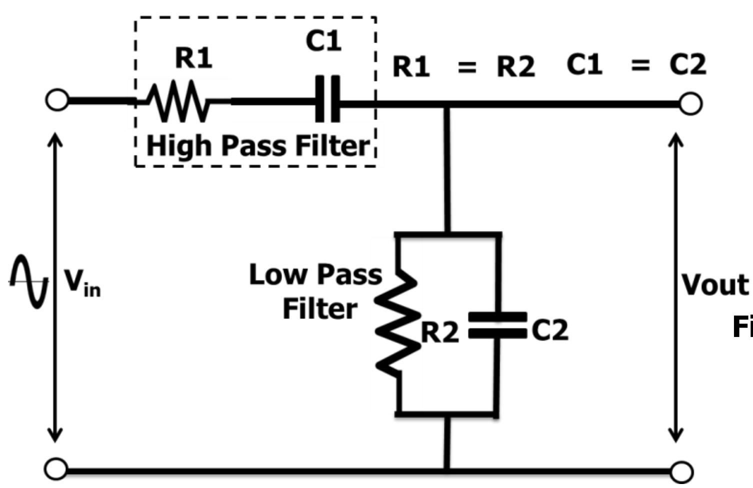


Fig 5.69

The bridge network is a high Q (very selective) second-order Band Pass Filter, at the selected frequency, f_o.

Theory of the Wien Bridge:

- At frequencies below resonance, C1 offers very high impedance and blocks any input signal. C1 acts like an open circuit. Since there is no input signal to the amplifier, there are no oscillations possible.
- At frequencies above resonance, C2 offers very low impedance and bypasses any input signal to ground. C1 acts like a short circuit. Since there is no input signal to the amplifier, there are no oscillations possible.
- At resonance frequency (f_o), C1 and C2 allow input signals to the amplifier where the output voltage, V_{OUT} reaches its maximum value.
- At the resonant frequency, the impedance of the capacitors equals the resistor values.
- It means Xc = R.
- Phase difference between the input and output equals zero degrees.
- The magnitude of the output voltage reaches its maximum value and this is equal to one third (1/3) of the input voltage.

The circuit is shown in fig 5.70

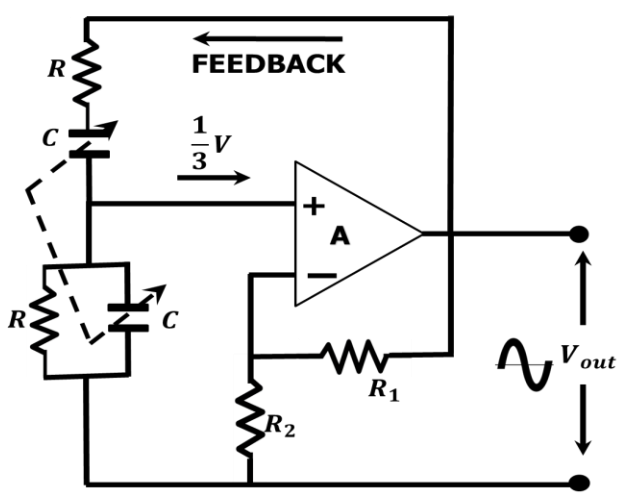


Fig 5.70

Wien Bridge Oscillator

Wien Bridge Oscillator Frequency

$$f_O = \frac{1}{2\pi RC}$$

The voltage gain of the amplifier circuit MUST be equal to or greater than three “Gain = 3” for oscillations to start because as we have seen above, the input is 1/3 of the output.

Limitations: Due to the open-loop gain limitations of operational amplifiers, frequencies above 1MHz are unachievable without the use of special high frequency op-amps.

Example

Determine the frequency of oscillations of a Wien Bridge Oscillator circuit having a resistor of 10kΩ and a capacitor of 0.01μF.

The frequency of oscillations for a Wien Bridge Oscillator is given as:

$$f_O = \frac{1}{2\pi RC}$$

$$f_O = \frac{1}{(2\pi \times 10000 \times 0.01 \times 10^{-6}} = 1590 \text{ Hz}$$

The Wien Bridge oscillator has excellent stability.

It has low distortion.

It is a very popular circuit as an audio frequency oscillator.

6.8 The Hartley Oscillator and Colpitts Oscillator

Both of these are LC class oscillators. The tank circuit (feedback circuit) uses inductors and capacitors. Both are sine wave RF Oscillators.

In **Colpitts** the tank circuit uses two centre-tapped capacitors in series which are in turn parallel with an inductor.

In **Hartley** the tank circuit uses two centre-tapped inductors in series which are in turn, parallel with a capacitor inductor.

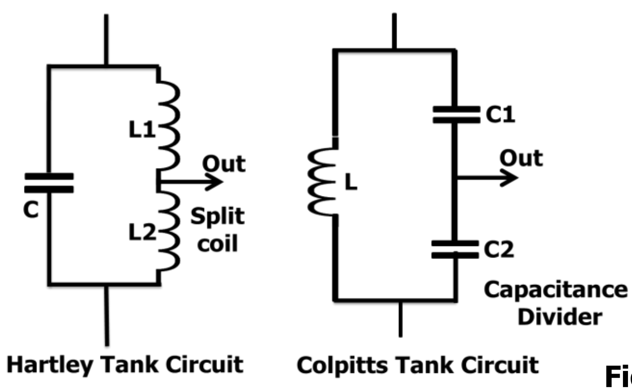


Fig 5.71

Oscillator Circuits

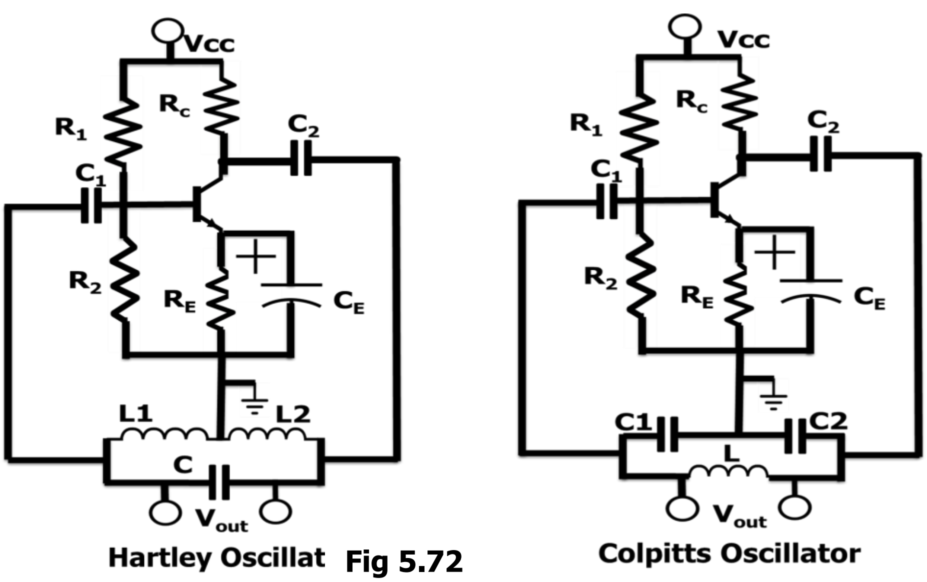


Fig 5.72

DESIGN:

BJT- Amplifier: Design a typical RC-Coupled BJT Amplifier. **A minimum gain of 2.9 is required to start oscillations.**

Design of a Hartley Oscillator for 100 KHz.

f_o = 100 kHz

Frequency of oscillation for Hartley Oscillator is given by:

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$ where L= L1 + L2 and [L1< L2]

$$C = \frac{1}{4\pi^2 f^2 L}$$

Let L1=100 µH, L2=1mH

Therefore, C=2.3nF

Design of a Colpitts Oscillator for 100 KHz.

$$f_o = \frac{1}{2\pi\sqrt{LC}}$$ where C_{eff}= (C1 C2) /(C1 + C2)

$$L = \frac{1}{4\pi^2 f^2 C_{eff}}$$

Let C1 = C2 =0.01 pF

Therefore L = 0.05066H

Colpitts Oscillator Op-amp Circuit

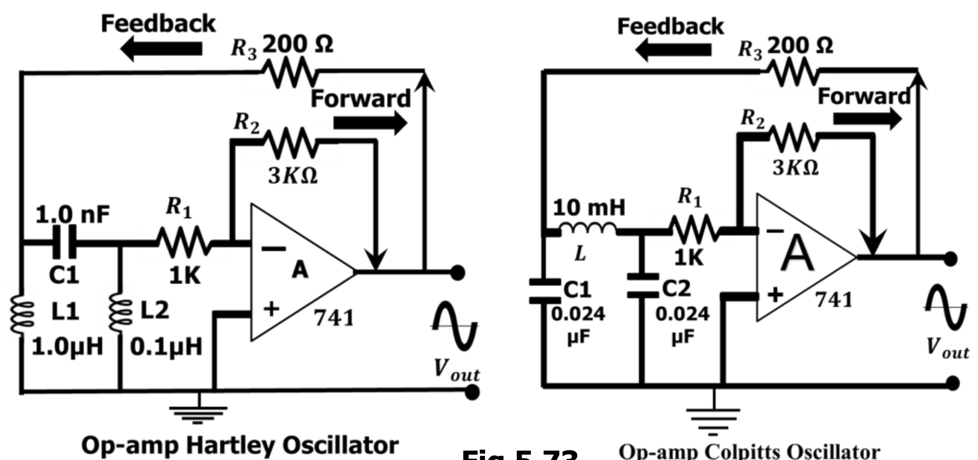


Fig 5.73

Colpitts Oscillator sinewaves are purer than Hartley oscillator's.

Colpitts oscillator can operate at very high frequencies.

6.9 BJT- CRYSTAL OSCILLATORS

What is a crystal oscillator?
A **crystal oscillator** is an electronic oscillator. It uses a component called piezoelectric crystal in its feedback network.

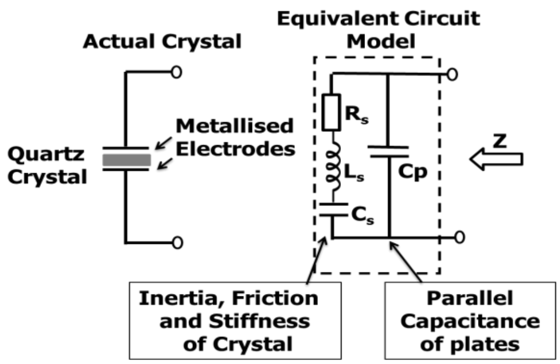


Fig 5.74

What is a piezoelectric crystal?
Also known as quartz crystal. It is a transducer**.** **Piezoelectricity** is the ability of certain materials to generate an AC (alternating current) voltage when subjected to mechanical stress or vibration, or to vibrate when subjected to an AC voltage, or both. When such a material is used in the tank circuit (feedback network) of an oscillator the frequency stability of the oscillator is very good

DESIGN:
Choose an appropriate crystal for the desired frequency of operation

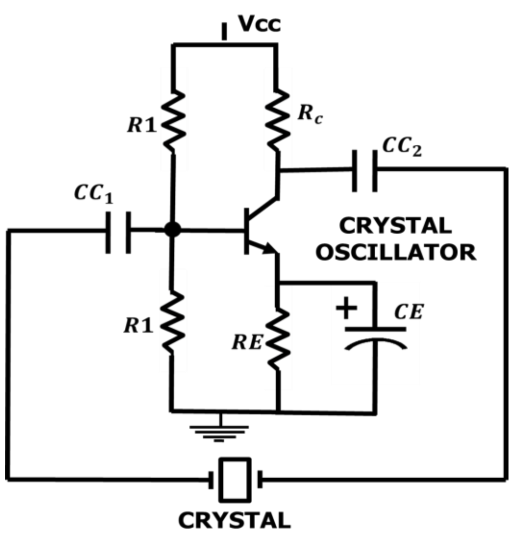


Fig 5.75

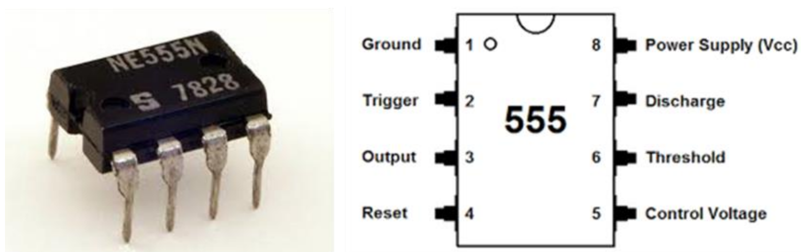
BJT- Amplifier: Design a proper RC-Coupled BJT Amplifier and connect the crystal of choice as shown. The circuit as per the circuit diagram shown. The circuit will oscillate at the crystal frequency

555 applications: Monostable & Astable operation using 555 timers

7.0 Astable and Monostable Multivibrator Using 555 IC

555 timer IC is a very popular IC used for Square wave genearation. Astable Multivibrator and the Monostable multivibrator are the important applications.

The pinout diagram for 555 IC is given in fig 5.76. The 8 pin package is very popular.



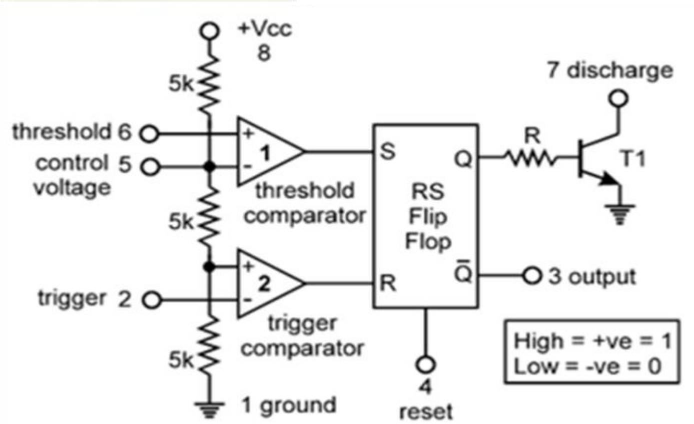


Fig 5.76

The pinout details are in the figure 5.76

<u>Pin Configuration and Functional diagram:-</u>

Pin 8. – Supply +Vcc, This is the power supply pin. **Let us assume V_{CC} = 6V**

Pin 1. – Ground, .

Pin 2. – Trigger: The negative input to the lower comparator. A negative pulse on this pin “sets” the internal Flip-flop from **LOW to HIGH**, when the voltage drops below 1/3 Vcc (2V in our example).

Pin 3. – Output, 555 output any TTL circuit. It can source up to 200mA of current at an output voltage of 1.5V. It is a terrific driver.

Pin 4. – Reset, When there is a LOW on this pin, output pin 3 goes low.

Pin 5. – Control Voltage, Internally it is set to 2/3 Vcc (4V in our example).It can be varied from 45% to 90% of the supply voltage. This variation causes the pulse width of the mono-stable to vary or the output frequency of the astable to vary. A 0.01 capacitor is connected to this pin and ground, to eliminate stray noise pick-up.

Pin 6. – Threshold: This is the positive input to the upper comparator. This pin connects directly to the RC timing circuit. The threshold voltage in 555 is at 2/3 Vcc (4V in our example). When the voltage at this input rises above this threshold value the output will go from **HIGH TO LOW** (Resets). In both astable and monostable mode the voltage across the timing capacitor is monitored through the Threshold input.
Pin 7. – Discharge, The discharge pin is connected directly to the Collector of an internal NPN transistor. When the voltage across the timing capacitor exceeds the threshold value (4V in our example), the timing capacitor is discharged through this input.and consequently the output at pin 3 goes “LOW”.

555 has three operating modes: Astable, Monostable and Bistable.

7.1 Astable Multivibrator: In astable multivibrator 555 produces a continuous square (rectangular) wave. No input or external trigger is required in this mode. It is self-oscillating.and free running..

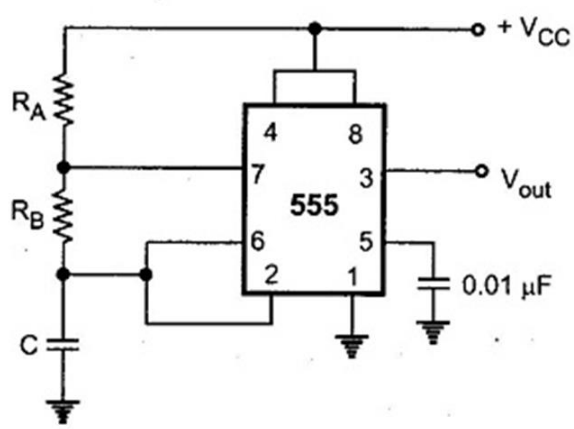


Fig 5.77

Astable Multivibrator

Astable mode is achieved by connecting the resistors R_A, R_B and the capacitor C to 555 as shown in the figure. Connections are to be made as shown in the circuit diagram.
The output produced by the astable circuit is not stable in both the HIGH and the LOW states and it continuously switches from one state to the other.
The timing (time period) during which the output is either high or low is determined by R1, R2 and C1.

Astable Multivibrator Operation

1. An astable 555 timer circuit contains an SR flip flop, two comparators, a **NPN driver transistor** and few discrete components like *resistors* and *capacitors* for its operation.
2. When the power supply is switched ON, the SR flip flop is **RESET**. Now, Q = 0. This forces the transistor to **cut-off** state.
3. The capacitor, C is free to charge and therefore will **charge** through R_A and R_B up to Vcc. with a time constant required for charging is equal to **(R_A + R_B) C.**
4. As the threshold voltage (capacitor voltage) becomes greater than 2/3 Vcc (4V in our example), comparator 1 will become HIGH. This will drive the S/R flip-flop to **SET.** Now, Q = 1. This forces the transistor to **saturation** state.
5. Capacitor C will find a discharging path thro the transistor and therefore **discharges.**

6. The discharging takes place through the resistor R_B. Hence the discharge time constant will be **R_BC.**
7. When the capacitor voltage becomes lower than 1/3 Vcc, comparator 1 will become LOW, S/R flip flop is **RESET** and the cycle repeats.

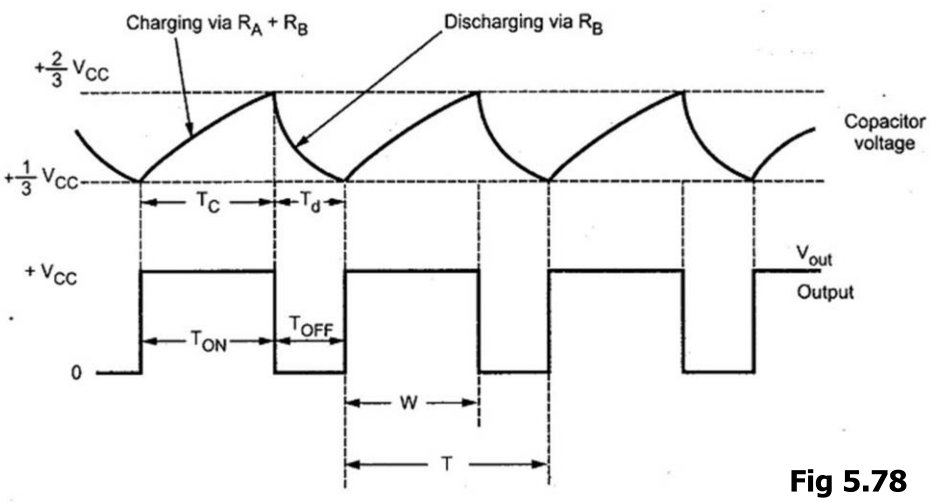


Fig 5.78

555 Astable : Charge-Discharge cycles

T_{ON} = 0.693 (R_A + R_B) C
T_{OFF} = 0.693 R_B C
$T = T_{ON} + T_{OFF}$
R_A and R_B are in ohms and C is in Farad

Duty cycle is the ratio of on time to the total time. Duty cycle = $\frac{T_{ON}}{T} = \frac{R_A+R_B}{(R_A+2R_B)}$

For 555 to operate as an astable multivibrator, it is necessary to *retrigger* the 555 IC after each and every cycle. This retriggering can be achieved by connecting the pin2 and the pin6 together.

Advantages & Disadvantages

- Simple to design and construct
- The output is a perfect square wave..
- 50% duty cycle is normally, difficult to achieve. This problem can be solved by inverting the output or by using a **diode** parallel to R

7.2 Monostable Multi Vibrator

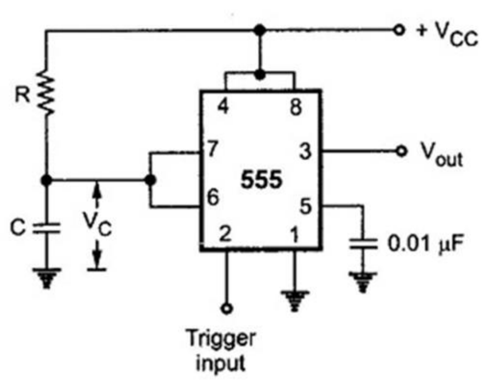


Fig 5.79

555 MONOSTABLE

1. A negative pulse is required at the trigger input of the multivibrator.
2. Comparator of the 555 timer detects this input and causes the flip-flop output to change from **LOW to HIGH**.
3. The transistor is driven to cut-off state..
4. The timing **capacitor** charges through resistor R1.
5. This charging will go on till voltage at pin6 of 555 timer reaches 2/3 Vcc.
6. When pin 6 reaches 2/3 Vcc, comparator output will move to **HIGH**.
7. This causes the flip-flop to go **LOW** and the driver
8. Now the Monostable multivibrator has to waiting for the other input trigger to repeat the entire process of operation.

Thus the pulse width W of a Monostable is

W = 1.1 RC

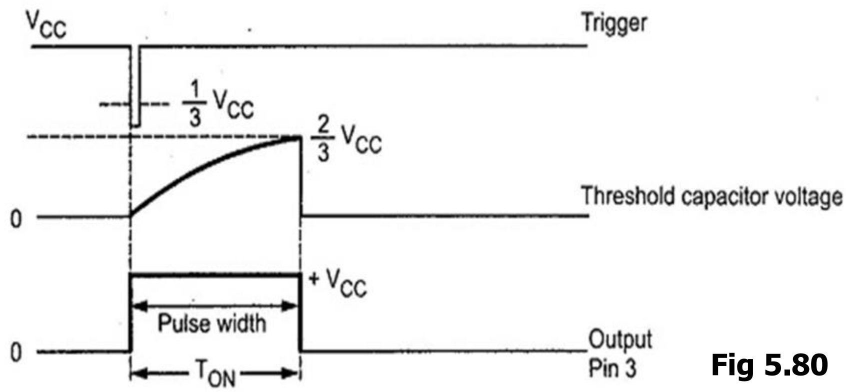


Fig 5.80

555 Monostable waveforms

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